

Automotive Electronics

Product Information

CG902-904 – Airbag System ICs



BOSCH
Invented for life



Product highlights

- ▶ All basic system functions integrated in one chip
- ▶ Adjustable to various system configurations thanks to 3 chip variants
- ▶ SW and HW compatible across all system configurations
- ▶ Supports a wide range of microcontroller families
- ▶ Fully automated diagnostic routines

Description

The CG902, -3 and -4 are integrated system ICs for Airbag applications with the possibility to realize a highly compact, two chip Airbag ECU consisting of a microcontroller and the system IC.

The CG90x combine power module, firing loop module, sensor interface module and a sophisticated safety module on a single chip

General functionality

- ▶ System Power Supply
- ▶ 8, 12 or 16 Firing Loops
- ▶ 2, 4 or 6 PSI5 Interfaces
- ▶ 10 AIN, 2 AIO Interfaces
- ▶ Safety Controller
- ▶ LIN/K-Line Interface

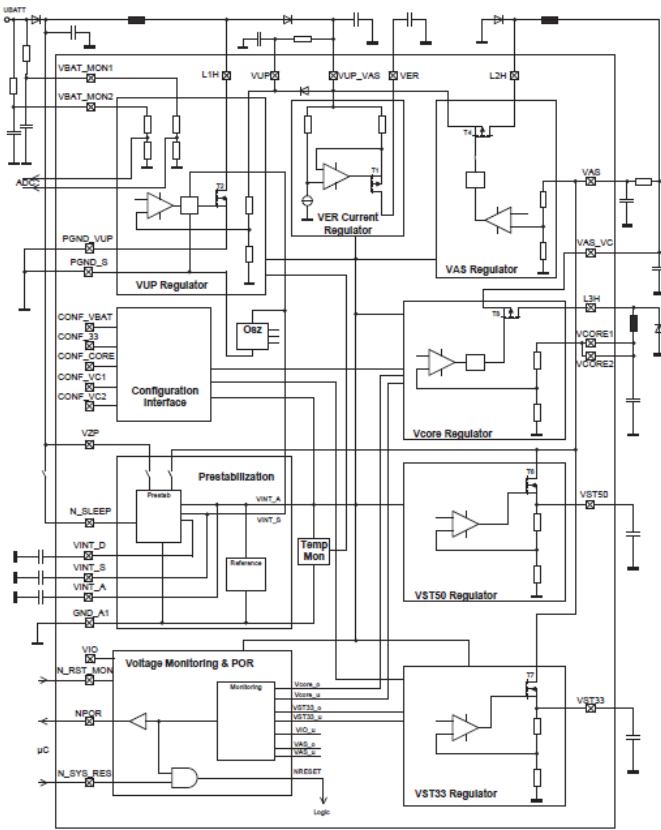
Customer benefits

- ▶ Maximum system safety thanks to a sophisticated safety concept with fully automated diagnostics
- ▶ Simple design-in due to hardware and software compatibility
- ▶ ISO –compliant design

Power module (features)

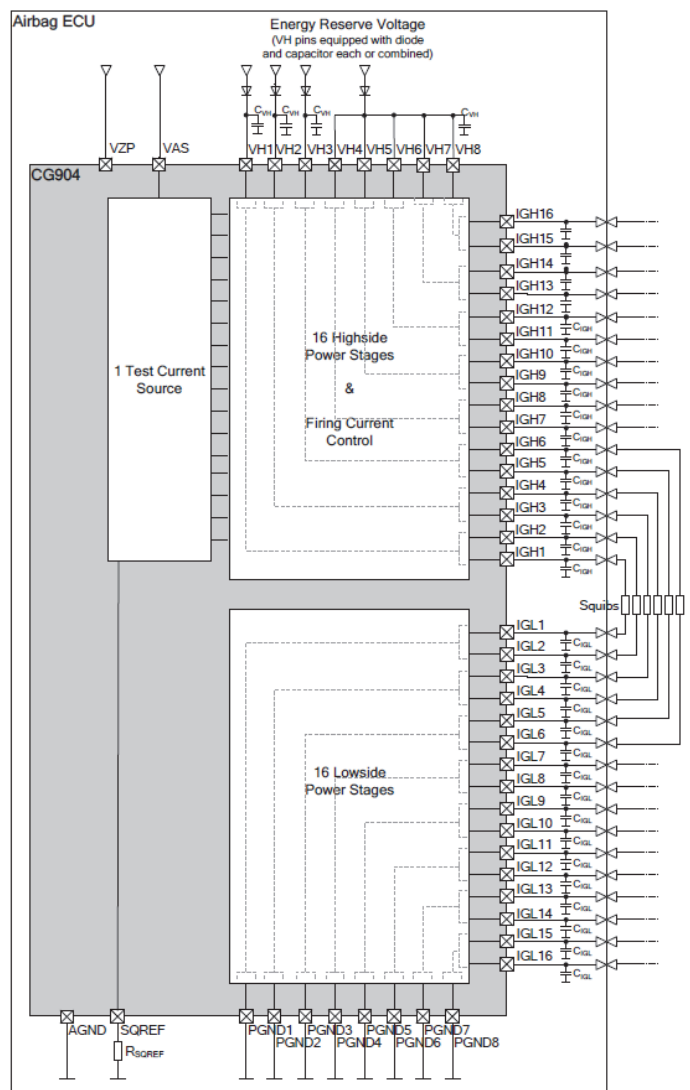
- ▶ Bandgap references for voltage regulation and voltage monitoring
- ▶ Internal reference current
- ▶ Internal oscillator with 1.875MHz
- ▶ VUP boost converter from VZP=5.2V...18V to VUP=33V/24V with 1.875MHz
- ▶ VER charger with programmable current levels
- ▶ VER test current functionality for capacitor and ESR test
- ▶ SPI control of supply test functions, supply status, VUP programming (output voltage and current limitation)
- ▶ Monitoring of battery voltage by dedicated VBAT_MON pins
- ▶ VAS buck converter VUP=10V...36V to VAS=6.7V with 1.875MHz
- ▶ VCORE buck converter VAS=6.7V to VCORE=3.3V/1.29V with 1.875MHz
- ▶ Programmable converter slope shaping and frequency jitter for improved EMC performance
- ▶ VST50 linear regulator VAS to VST50=5V (CAN supply, ECU internal sensors)
- ▶ VST33 linear regulator VAS to VST33=3.3V (analog & digital supply)
- ▶ VCORE/VST33 configuration by dedicated CONF pins
- ▶ Bandgap references for voltage regulation and voltage
- ▶ Voltage monitoring of low voltage pins and power-on reset logic
- ▶ Sleep mode control with $I_{sleep} \leq 60\mu A$
- ▶ Over-temperature shut down of VUP converter

Power module (block diagram)



- ▶ automatic high precision loop diagnosis:
 - ▶ squib resistance measurement for determining the ohmic part
 - ▶ test current level and duration for squib resistance measurement programmable via SPI
 - ▶ squib detection test for detecting an open load
 - ▶ safe power stage diagnosis test
 - ▶ connector capacitor diagnosis
- ▶ maximum distance between highside and lowside power stages due to cross placement on chip

Firing loop module (block diagram)



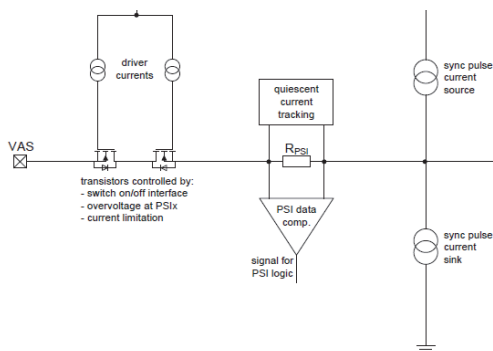
Firing loop module (features)

- ▶ 16 firing loops (CG904), 12 firing loops (CG903) or 8 firing loops (CG902)
- ▶ highside and lowside power stages short-circuit protected
- ▶ hardware switch-off of power stages
- ▶ general disable for power stages
- ▶ special disable of dedicated power stages
- ▶ independent control and power supply of highside and lowside power stages
- ▶ different firing modes programmable by SPI:
 - ▶ static mode I: 1.85 A for 0.7 ms
 - ▶ static mode II: 1.75 A for 0.5 ms
 - ▶ static mode III: 1.2 A for 2 ms
 - ▶ dynamic mode V: 1.75 A for 0.7 ms, automatic extension to 1.2 A for 2.0 ms possible
 - ▶ dynamic mode VI: 1.5 A for 1.5 ms, automatic extension up to 3.0 ms possible
- ▶ high resolution firing current counters (40 kHz, 7 bit), independent of firing current
- ▶ automatic high precision loop diagnosis:
 - ▶ short detection on all IGH and IGL pins to detect short circuits or leakage resistors to battery or ground
 - ▶ cross coupling test to detect short circuits between the firing loops
 - ▶ VH voltage measurement and SVR diagnosis by the internal ADC

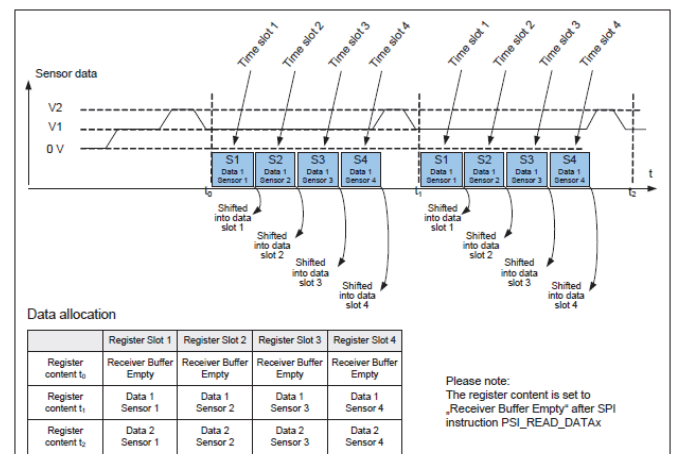
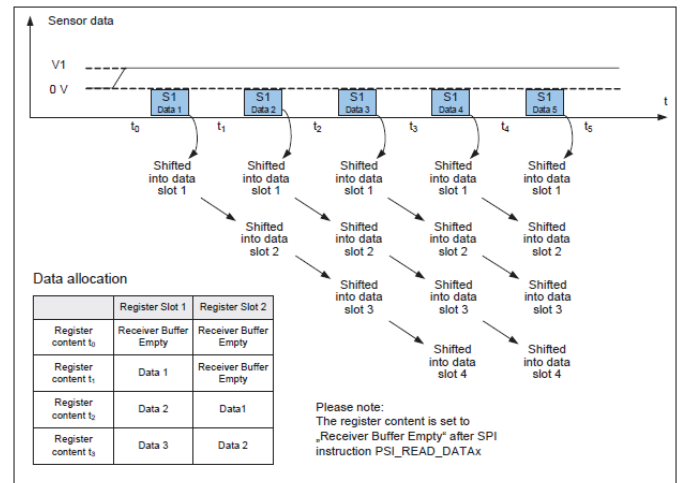
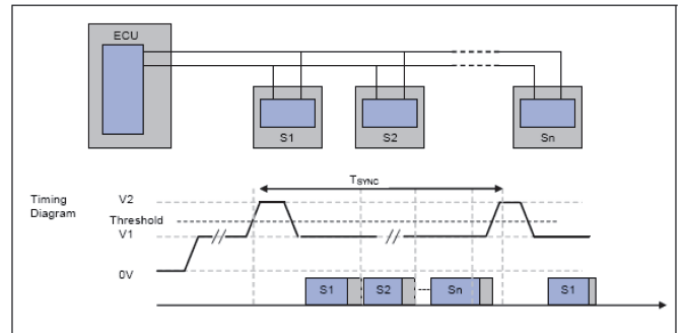
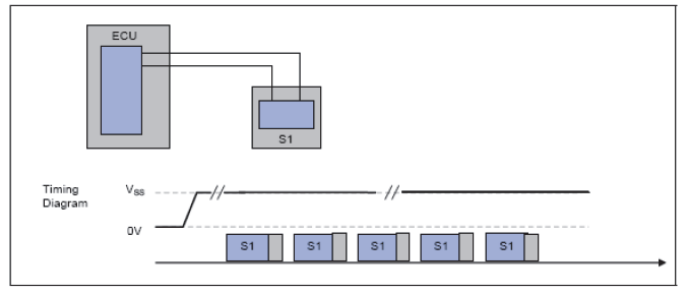
Interface module (features)

- ▶ 32bit SPI, 10MHz, 10 bit SPI instruction
- ▶ programming enable bit (pe)
- ▶ 16 bit input and output data
- ▶ 3 bit CRC for input and output signal
- ▶ 6 general status flags
- ▶ sensor data flag (S)
- ▶ 5 bit safety ID / 5 additional status flags
- ▶ global status flag (gs)
- ▶ 6 PSI5 interfaces integrated
 - ▶ Asynchronous (PSI5-A) and synchronous (PSI5) operation
 - ▶ Point-to-point and bus mode
 - ▶ 3 different data transmission modes selectable (83.3 kbps, 125 kbps, 189 kbps)
 - ▶ Operation with up to 4 sensors per interface (189 kbps data transmission)
 - ▶ Operation with up to 3 sensors per interface (125 kbps data transmission)
 - ▶ Operation with up to 2 sensors per interface (83.3 kbps data transmission)
 - ▶ Uni- and bidirectional communication
 - ▶ Two-wire interface (combined lines for supply and data transmission)
 - ▶ Manchester-coded digital data transmission
 - ▶ 10 bit data frame
 - ▶ 3 bit CRC mode or single bit parity mode selectable
 - ▶ Integrated comparator functionality for voltage monitoring of sensor channels
 - ▶ Safety identifier programmable for each channel and time slot
 - ▶ Integrated resistor for communication current detection
 - ▶ 3 different PSI sync pulse trigger modes (pin, SPI, automatic timing)
 - ▶ PSI sync pulse control
 - ▶ PSI quiescent current tracking
 - ▶ PSI comparator threshold control
 - ▶ VAS reverse current protection
 - ▶ PSI data path consistency check
 - ▶ Configurable handling of data words extending across time slot limits
 - ▶ Cross-coupling diagnosis
 - ▶ Automatic PSI deactivation in case of short-to-ground

PSI5 interface (block diagram)



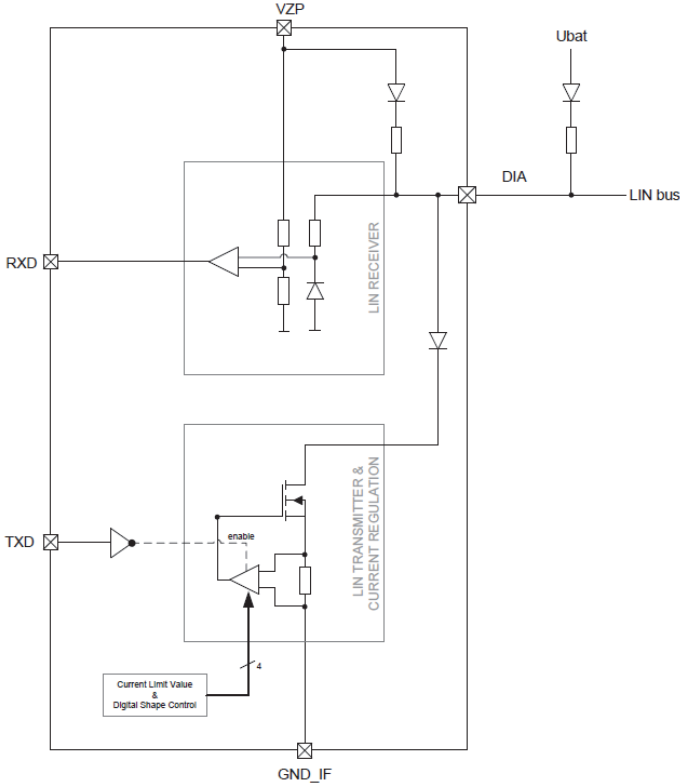
Transmission of sensor data



LIN/K-Line (features)

- ▶ LIN interface according to 2.1 standard
- ▶ General purpose mode as low side switch (current controlled)
- ▶ PWM control with 100, 200, 266, or 400Hz possible
- ▶ Short and timeout protected

LIN/K-Line (features)

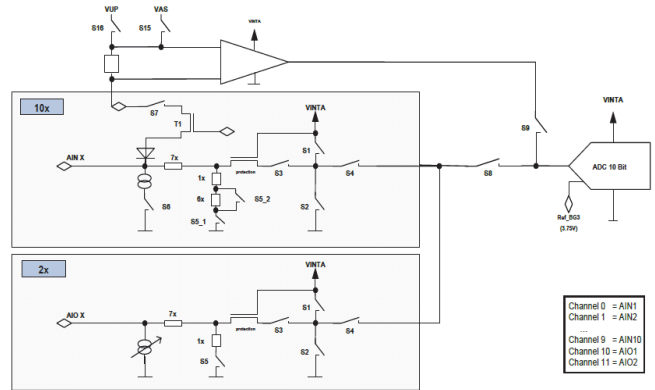


AIN (features)

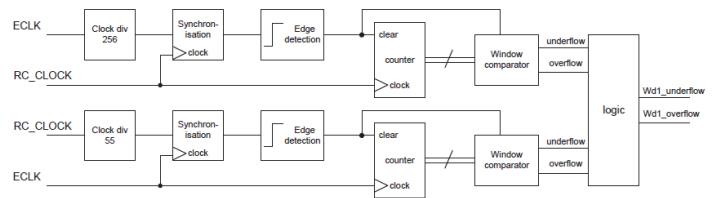
- ▶ Programmable VAS/VUP voltage at all AIN outputs (AIN1...10)
- ▶ Programmable current source from 3mA up to 18mA in fixed VAS current mode and 1.5mA up to 9mA in fixed VUP current mode
- ▶ Programmable voltage source with an ability to drive current of 30mA in fixed VAS voltage mode (hall mode) and 10mA in fixed VUP voltage mode
- ▶ Reference current generation
- ▶ Analog current measurement in fixed current and fixed voltage mode possible

AIO (features)

- ▶ AIO interfaces as programmable current sinks
- ▶ PWM control between 0 and 100% at 100, 200, 266, or 400Hz possible
- ▶ Programmable warning lamp mode
- ▶ Short detection



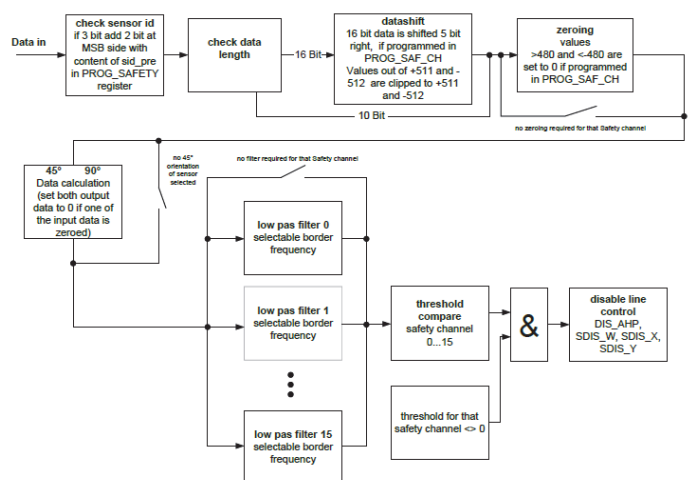
Safety module - 3 level Watchdog



Monitor SPI for data plausibility check

| <i>n</i> | <i>keyword hex</i> | <i>response hex</i> |
|----------|--------------------|---------------------|
| 1 | 2020 | E106 |
| 2 | FDFD | 9671 |
| 3 | 8A8A | 4BAC |
| 4 | 5757 | 3CDB |
| 5 | ECEC | D235 |
| 6 | 3131 | A542 |
| 7 | 4646 | 789F |
| 8 | 9B9B | 0FE8 |

Programmable filter and threshold comparator



Pin description list

| pin | name | direction | description | module |
|-----|-----------|-----------|--|--------|
| 1 | n.c. | open | not connected | - |
| 2 | VAS_VC | power | power supply for VCORE | POM |
| 3 | VAS | power | stabilized analog supply 6,7 V | POM |
| 4 | CONF_33 | input | configuration 3,3V regulator | POM |
| 5 | CONF_CORE | input | configuration core regulator | POM |
| 6 | CONF_VC1 | input | configuration core regulator voltage | POM |
| 7 | CONF_VC2 | input | configuration core regulator voltage | POM |
| 8 | L2H | power | coil 2 VAS high side connection | POM |
| 9 | VUP_VAS | power | power supply for VAS | POM |
| 10 | VUP | power | up converter output | POM |
| 11 | VER | power | energy reserve output | POM |
| 12 | CONF_VBAT | input | configuration boost converter on threshold | POM |
| 13 | VBAT_MON1 | input | battery voltage monitoring | POM |
| 14 | L1H | power | coil 1 VUP high side connection | POM |
| 15 | PGND_VUP | ground | ground | POM |
| 16 | VINT_S | power | internal supply for switch regulator 4,75V | POM |
| 17 | PGND_S | ground | ground | POM |
| 18 | VINT_A | power | internal analog supply 4,75V | POM |
| 19 | CONF_RES | input | configuration reset behavior | SAM |
| 20 | VBAT_MON2 | input | battery voltage monitoring | POM |
| 21 | N_POR | output | power on reset | POM |
| 22 | N_RST_MON | input | external reset monitoring | POM |
| 23 | ECLK | input | system clock 4MHz | System |
| 24 | VIO | power | internal I/O supply 3,3V | POM |
| 25 | SCK | input | SPI clock input | SPI |
| 26 | SI | input | SPI slave input | SPI |
| 27 | SO | bi-dir | SPI slave output (SO monitor internal) | SPI |
| 28 | N_CS_MON | input | chip select monitor | SPI |
| 29 | N_CS | input | chip select ASIC | SPI |
| 30 | TXD | input | transmit data | LIN |
| 31 | RXD | output | receive data | LIN |
| 32 | GND_S1 | ground | ground | - |

| pin | name | direction | description | module |
|-----|-----------|-----------|--|--------|
| 65 | SDIS_S | bi-dir | special disable switch evaluation | SAM |
| 66 | SDIS_W | bi-dir | special disable w-channel | SAM |
| 67 | SDIS_Y | bi-dir | special disable y-channel | SAM |
| 68 | SDIS_X | bi-dir | special disable x-channel | SAM |
| 69 | GND_A2 | ground | ground | - |
| 70 | SVR_DIAG | dedicated | input test sink for SVR test | FLM |
| 71 | AIO1 | dedicated | analog I/O | AIO |
| 72 | AIO2 | dedicated | analog I/O | AIO |
| 73 | AIN1 | dedicated | analog input | AIN |
| 74 | AIN3 | dedicated | analog input | AIN |
| 75 | AIN5 | dedicated | analog input | AIN |
| 76 | AIN7 | dedicated | analog input | AIN |
| 77 | AIN9 | dedicated | analog input | AIN |
| 78 | PSI1 | dedicated | PSI channel | PSI |
| 79 | PSI3 ** | dedicated | PSI channel | PSI |
| 80 | PSI5 ** | dedicated | PSI channel | PSI |
| 81 | VSYN | power | supply voltage for PSI sync pulse | PSI |
| 82 | PSI6 ** | dedicated | PSI channel | PSI |
| 83 | PSI4 ** | dedicated | PSI channel | PSI |
| 84 | PSI2 | dedicated | PSI channel | PSI |
| 85 | SQREF | dedicated | squb reference resistor | FLM |
| 86 | AIN10 | dedicated | analog input | AIN |
| 87 | AIN8 | dedicated | analog input | AIN |
| 88 | AIN6 | dedicated | analog input | AIN |
| 89 | AIN4 | dedicated | analog input | AIN |
| 90 | AIN2 | dedicated | analog input | AIN |
| 91 | AOUT | output | analog output multiplexer | System |
| 92 | DIS_ALP | bi-dir | disable all low side power stages | FLM |
| 93 | N_SYS_RES | input | system reset | System |
| 94 | DIS_SHP | input | disable special high side power stages | FLM |
| 95 | DIS_AHP | bi-dir | disable all high side power stages | FLM |
| 96 | GND_S2 | ground | ground | - |

** pin is not connected in CG902

*** pin is not connected in CG903/CG902

| pin | name | direction | description | module |
|-----|-----------|-----------|--------------------------------------|--------|
| 33 | N_SLEEP | input | sleep control | POM |
| 34 | VZP | power | central protected supply | POM |
| 35 | DIA | dedicated | LIN bus | LIN |
| 36 | GND_IF | ground | ground | LIN |
| 37 | PSI_SYNC | input | PSI sync pulse synchronization | PSI |
| 38 | TESTM | input | ASIC test mode activation | System |
| 39 | VINT_D | power | internal digital supply 1,8V | POM |
| 40 | GND_D | ground | ground | POM |
| 41 | IGH2 | dedicated | high side power stage 2 | FLM |
| 42 | IGL4 | dedicated | low side power stage 4 | FLM |
| 43 | VH1 | power | supply voltage high side power stage | FLM |
| 44 | PGND2 | ground | power stage ground | FLM |
| 45 | IGH1 | dedicated | high side power stage 1 | FLM |
| 46 | IGL3 | dedicated | low side power stage 3 | FLM |
| 47 | IGH6 | dedicated | high side power stage 6 | FLM |
| 48 | IGL8 | dedicated | low side power stage 8 | FLM |
| 49 | VH3 | power | supply voltage high side power stage | FLM |
| 50 | PGND4 | ground | power stage ground | FLM |
| 51 | IGH5 | dedicated | high side power stage 5 | FLM |
| 52 | IGL7 | dedicated | low side power stage 7 | FLM |
| 53 | IGH10 * | dedicated | high side power stage 10 | FLM |
| 54 | IGL12 * | dedicated | low side power stage 12 | FLM |
| 55 | VH5 * | power | supply voltage high side power stage | FLM |
| 56 | PGND6 * | ground | power stage ground | FLM |
| 57 | IGH9 * | dedicated | high side power stage 9 | FLM |
| 58 | IGL11 * | dedicated | low side power stage 11 | FLM |
| 59 | IGH14 *** | dedicated | high side power stage 14 | FLM |
| 60 | IGL16 *** | dedicated | low side power stage 16 | FLM |
| 61 | VH7 *** | power | supply voltage high side power stage | FLM |
| 62 | PGND8 *** | ground | power stage ground | FLM |
| 63 | IGH13 *** | dedicated | high side power stage 13 | FLM |
| 64 | IGL15 *** | dedicated | low side power stage 15 | FLM |

* pin is not connected in CG902

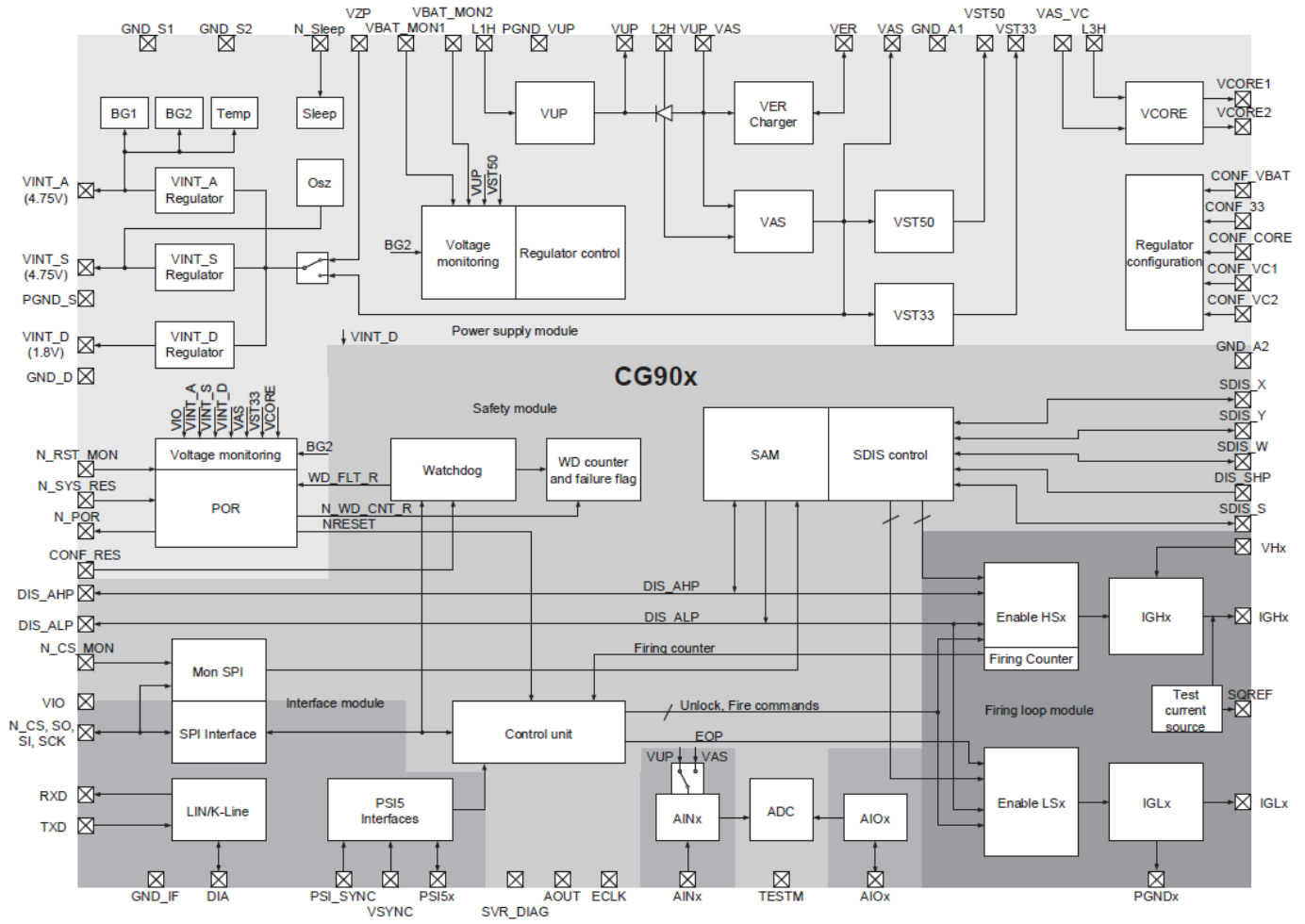
** pin is not connected in CG903/CG902

| pin | name | direction | description | module |
|-----|-----------|-----------|--------------------------------------|--------|
| 97 | IGL14 *** | dedicated | low side power stage 14 | FLM |
| 98 | IGH16 *** | dedicated | high side power stage 16 | FLM |
| 99 | PGND7 *** | ground | power stage ground | FLM |
| 100 | VH8 *** | power | supply voltage high side power stage | FLM |
| 101 | IGL13 *** | dedicated | low side power stage 13 | FLM |
| 102 | IGH15 *** | dedicated | high side power stage 15 | FLM |
| 103 | IGL10 * | dedicated | low side power stage 10 | FLM |
| 104 | IGH12 * | dedicated | high side power stage 12 | FLM |
| 105 | PGND5 * | ground | power stage ground | FLM |
| 106 | VH6 * | power | supply voltage high side power stage | FLM |
| 107 | IGL9 * | dedicated | low side power stage 9 | FLM |
| 108 | IGH11 * | dedicated | high side power stage 11 | FLM |
| 109 | IGL6 | dedicated | low side power stage 6 | FLM |
| 110 | IGH8 | dedicated | high side power stage 8 | FLM |
| 111 | PGND3 | ground | power stage ground | FLM |
| 112 | VH4 | power | supply voltage high side power stage | FLM |
| 113 | IGL5 | dedicated | low side power stage 5 | FLM |
| 114 | IGH7 | dedicated | high side power stage 7 | FLM |
| 115 | IGL2 | dedicated | low side power stage 2 | FLM |
| 116 | IGH4 | dedicated | high side power stage 4 | FLM |
| 117 | PGND1 | ground | power stage ground | FLM |
| 118 | VH2 | power | supply voltage high side power stage | FLM |
| 119 | IGL1 | dedicated | low side power stage 1 | FLM |
| 120 | IGH3 | dedicated | high side power stage 3 | FLM |
| 121 | GND_A1 | ground | ground | - |
| 122 | VST33 | power | stabilized supply 3,3 V | POM |
| 123 | VST50 | power | stabilized supply 5,0 V | POM |
| 124 | n.c. | open | not connected | - |
| 125 | L3H | power | coil 3 VCORE high side connection | POM |
| 126 | n.c. | open | not connected | - |
| 127 | VCORE1 | power | core converter output | POM |
| 128 | VCORE2 | power | core converter output | POM |

* pin is not connected in CG902

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CG90x block diagram



Regional sales contacts

| | |
|------------|--|
| Europe | bosch.semiconductors@de.bosch.com |
| USA/Canada | bosch.semiconductors@us.bosch.com |
| Japan | bosch.semiconductors@jp.bosch.com |
| China | bosch.semiconductors@cn.bosch.com |
| Korea | bosch.semiconductors@kr.bosch.com |

www.bosch-semiconductors.com
www.bosch-sensors.com

Robert Bosch GmbH

AE/MBC
Postfach 13 42
72703 Reutlingen
Germany

www.bosch.com