Automotive Electronics

Product Information
8-Loop Firing IC – CG988

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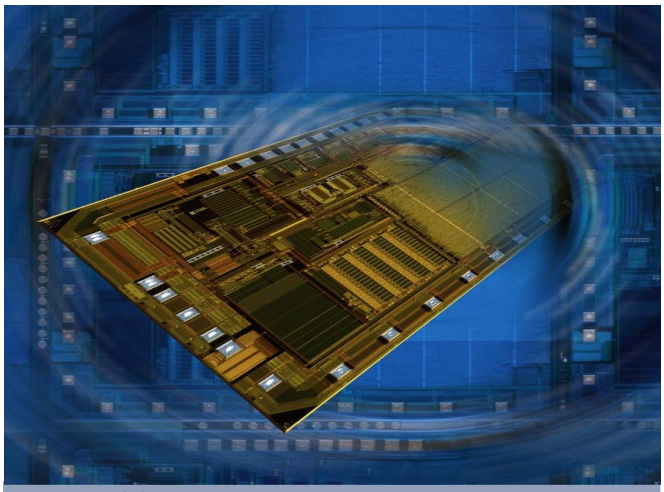
Invented for life



8-Loop Firing IC

Customer benefits:

- Excellent system know-how
- Smart concepts for system safety
- Secured supply
- Long- term availability of manufacturing processes and products
- QS9000 and ISO/TS16949 certified

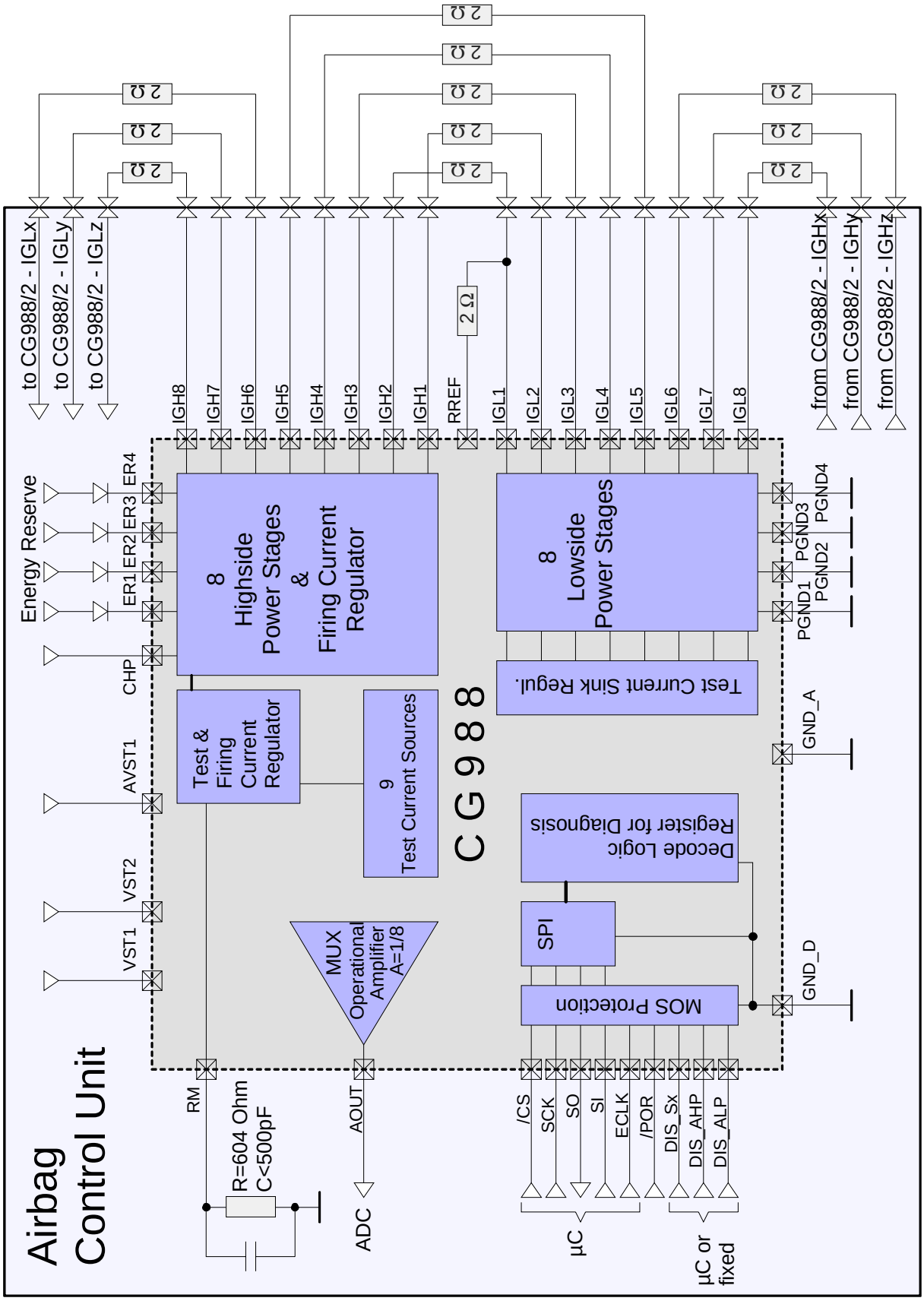
Following the successful implementation of the CG685/CG687 Quad- and Dual Firing Loop ICs, Bosch Automotive Electronics will move along with the introduction of a highly integrated version of a firing IC with 8 fully integrated squib driver channels for DC firing. The CG988 is being designed by utilizing leading-edge automotive ASIC processes with 0.8•m feature size. The superior performance with respect to precision and reliability and the well-proven safety concept of its predecessors will be combined with a variety of new features as required by the quickly evolving next generations of electronic safety systems.

Features

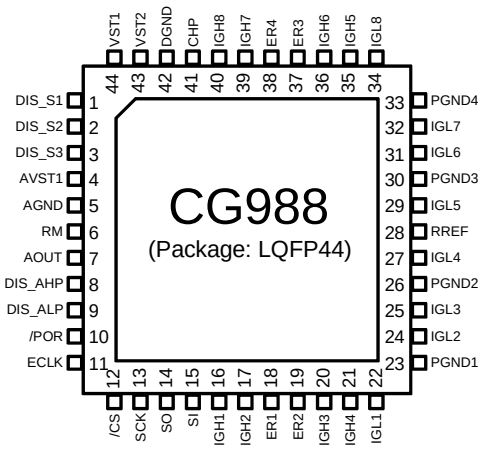
- Optimized firing concept with 2 firing modes for efficient energy management
- Firing current >2A for 3ms, single pulse
- Energy reserve voltage up to 35V
- Full cross coupling capability (highside and lowside drivers placed on different ASICs)
- Firing current counter, 4 bit per firing loop
- High precision firing loop diagnostics (shorts, leakage, squib resistance)
- 26 channel analog multiplexer with tristate mode to monitor squib pins and supply voltages
- Sophisticated safety concept (power-on reset, disable pins for highside and for lowside stages, redundant firing path circuitry)
- 3 safety disable pins to lock 3 groups of up to 8 firing-loops
- All functions controlled via 8MHz, 16 bit bi-directional SPI
- 5V/3.3V systems compatibility
- QFP44 package

Application example

(Example for cross coupling of firing loops 6-8 shown)



PIN configuration



PIN description

No	Name	Class.	Description	Comments / Recommended Circuit
1	DIS_S1	In	Special disable of firing loops 1-8, Group 1	µC or fixed
2	DIS_S2	In	Special disable of firing loops 1-8, Group 2	µC or fixed
3	DIS_S3	In	Special disable of firing loops 1-8, Group 3	µC or fixed
4	AVST1	Supply	Analog stabilised voltage input	5V
5	AGND	Supply	Analog ground	GND
6	RM	In	Test current adjust	604Ω ± 1%, C<500pF
7	AOUT	Out	Analog multiplexer output	µC, A/D
8	DIS_AHP	In	Disable all highside power stages	µC
9	DIS_ALP	In	Disable all lowside power stages	µC
10	/POR	In	Power on reset, active low	RESET circuit
11	ECLK	In	External clock, 2 MHz	µC, Clock 2MHz
12	/CS	In	Chip select	µC, SPI
13	SCK	In	Serial clock, 8MHz	µC, SPI, Clock 8MHz max.
14	SO	Out	Slave out	µC, SPI
15	SI	In	Slave in	µC, SPI
16	IGH1	Out	Igniter loop high, channel 1	Squib loop 1, highside
17	IGH2	Out	Igniter loop high, channel 2	Squib loop 2, highside
18	ER1	Supply	Energy reserve voltage firing loop 1,2	33V±2V, energy reserve
19	ER2	Supply	Energy reserve voltage firing loop 3,4	33V±2V, energy reserve
20	IGH3	Out	Igniter loop high, channel 3	Squib loop 3, highside
21	IGH4	Out	Igniter loop high, channel 4	Squib loop 4, highside
22	IGL1	In	Igniter loop low, channel 1	Squib loop 1, lowside
23	PGND1	Supply	Power ground firing loop 1,2	GND
24	IGL2	In	Igniter loop low, channel 2	Squib loop 2, lowside
25	IGL3	In	Igniter loop low, channel 3	Squib loop 3, lowside
26	PGND2	Supply	Power ground firing loop 3,4	GND
27	IGL4	In	Igniter loop low, channel 4	Squib loop 4, lowside
28	RREF	Out	Reference resistor	Expected total firing loop resistance
29	IGL5	In	Igniter loop low, channel 5	Squib loop 5, lowside
30	PGND3	Supply	Power Ground Firing Loop 5,6	GND
31	IGL6	In	Igniter loop low, channel 6	Squib loop 6, lowside
32	IGL7	In	Igniter loop low, channel 7	Squib loop 7, lowside
33	PGND4	Supply	Power ground riring loop 7,8	GND
34	IGL8	In	Igniter loop low, channel 8	Squib loop 8, lowside
35	IGH5	Out	Igniter loop high, channel 5	Squib loop 5, highside
36	IGH6	Out	Igniter loop high, Channel 6	Squib loop 6, highside
37	ER3	Supply	Energy reserve voltage firing Loop 5,6	33V±2V, energy reserve
38	ER4	Supply	Energy reserve voltage firing Loop 7,8	33V±2V, energy reserve
39	IGH7	Out	Igniter loop high, channel 7	Squib Loop 7, highside
40	IGH8	Out	Igniter loop high, channel 8	Squib Loop 8, highside
41	CHP	Supply	Charge pump voltage	VERx+7V
42	DGND	Supply	Digital ground	GND
43	VST2	Supply	Digital 3.3V/5V stabilized voltage input	3.3V/5V (according to µC)
44	VST1	Supply	Digital 5V stabilized voltage input	5V

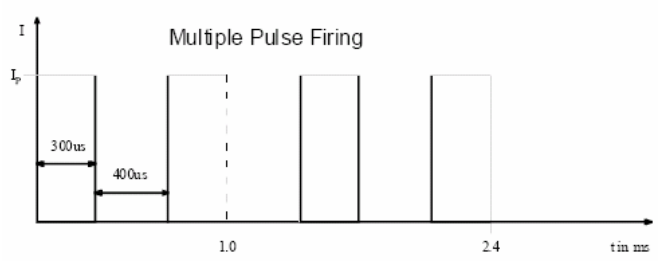
Dual Firing Mode Concept

The CG988 operates in two different firing modes depending on the energy reserve voltage at pins ER1-ER4 (the proper firing mode is set by the CG988 and is not accessible by SPI command). Starting the firing sequence with an energy reserve voltage of 35V, CG988 fires with multiple pulses at high current level for an efficient energy management. The nominal firing current is 3A. As the energy reserve voltage falls beyond $V_{ER(nom)}$=23.5V the second mode (single pulse firing mode) is enabled with a minimal firing current of 2A. The reduced firing current for single pulse ensures full energy for the squib down to low energy reserve voltages. The pulse mode of the selected loop is determined by the ASIC and remains unchanged during the complete firing sequence. The gain in efficiency in comparison to conventional DC firing concepts is in the range of 20 to 25 percent. The dual firing mode concept operates without any additional effort by µC.

To ensure an optimized firing of both high energy and low energy squibs two different time frames are defined: 1ms for low energy squibs and 2.5ms for their high energy counterparts. The firing sequence can be extended up to 3ms with full short circuit protection.

*R_{Squib}=2Ω

Multiple pulse firing

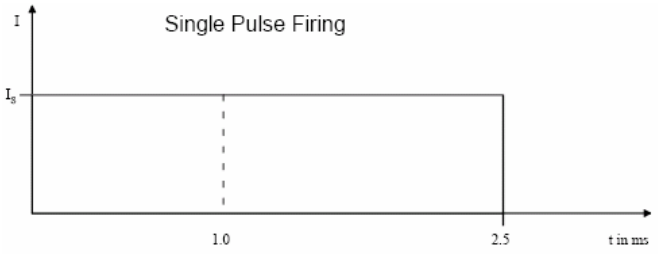


$V_{ER(nom)}$ • 23.5 V

I_P: 2.55A ... 3.45A, nominal 3.0A

Firing time adjustable by software.

Single pulse firing



$V_{ER(nom)}$ <23.5 V

I_S: 2.0A ... 2.8A, nominal 2.4A

Firing time adjustable by software.

Maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltages	V_{ER1-2}	-0.3		36	V
	V_{CHP}	-0.3		36	V
	V_{VST1}	-0.3		7	V
	V_{AVST1}	-0.3		7	V
	V_{VST2}	-0.3		7	V
Power ground	$V_{PGND1..2}$	-0.3		0.3	V
Digital ground	V_{DGND}	-0.3		0.3	V
Firing loops, static	$V_{IGH1..4}$	-0.3		36	V
	$V_{IGL1..4}$	-0.3		36	V
	V_{RREF}	-0.3		36	V
Junction temperature	T_j	-40		150	°C
Operating temperature	T_{amb}	-40		105	°C
ESD classification Human body model - All pins except VST1, VST2 - VST1, VST2	V_{HBM}	 -2000 -800		 2000 800	 V V

Electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltages	V_{ER1}	10		35	V
	V_{ER2-4}	5.2		35	V
	V_{CHP}	V_{ERmin}+7		35	V
	V_{VST1}	4.7	4.9	5.1	V
	V_{AVST1}	4.7	4.9	5.1	V
	V_{VST2}	3.1/4.7*	3.3/4.9*	3.5/5.1*	V

Parameter	Symbol	Min.	Typ.	Max.	Unit
Current reference (AVST1=4.9V)	R_{RM}		604		Ω
	I_{RM}	-4%	2	4%	mA
Test current source					
Ratio test/ reference current, I_{RM}=2mA	I_{RREF}/I_{RM}	18.5	19.75	21	
Tracking of test current source,0≤V_{IGH}≤0.5V	I_{IGHx}/I_{IGHy}	0.99	1.00	1.1	
Test current sink					
Saturation voltage, I_{IGL}=40mA	V_{IGL}	10	20	40	mV
Tracking of saturation voltage, lowside	V_{IGLx}/V_{IGLy}	-20%	1	20%	
Current limitation, V_{IGL}<18V, t<3ms	I_{IGL}	60	120	180	mA
Voltage divider at IGLx, IGHx					
Pull up resistor for leakage tests	R_{IGHx},R_{IGLx}	6	12	20	kΩ
Pull down resistor for leakage tests	R_{IGHx},R_{IGLx}	3	6	10	kΩ
Quiescent potential	V_{IGHx},V_{IGLx}	-5%	AVST1/3	5%	V
Highside power stage					
Firing current (t_{ON} ≤ 3ms, V_{ER} ≤ 35V)					
Switching voltage between firing modes	V_{SW}	22	23.5	25	V
Pulse mode, V_{ER}>V_{SW}	$-I_{IGHx}$	2.55	3.0	3.45	A
Single pulse mode, V_{ER}<V_{SW}	$-I_{IGHx}$	2.0	2.4	2.8	A
Duty cycle, pulse mode, error<1%		41.5	43	50	%
Drain-source on-state resistance (T_J≤105°C, I_{DS}=0.5A)	$R_{DS(on)}$		0.8	1.2	Ω
Drain-source voltage (T_J≤105°C, I_{DS}=2A)	$V_{DS(min)}$			3	V
Lowside power stage					
Firing current (t_{ON} ≤ 2.5ms, V_{ER} ≤ 35V)					
Current load capacity (T_J≤105°C)	I_{IGLx}	3.5			A
Drain-source on-state resistance	$R_{DS(on)}$		0.6	1.0	Ω
(T_J≤105°C, I_{DS}=0.5A)					
Drain-source voltage (T_J≤105°C, I_{DS}=2A)	$V_{DS(min)}$			3	V
Firing current detection level					
V_{ER}-V_{IGH}>5V					
Multiple pulse mode	$I_{FDET(MP)}$	1.5		$I_{REG(MP)}$	A
Single pulse mode	$I_{FDET(SP)}$	1.2		$I_{REG(SP)}$	A

* V_{VST2} in 5V System environment

** measured with reduced accuracy; guarantied by design

Contact

Robert Bosch GmbH
Sales Semiconductors
Postbox 13 42
72703 Reutlingen
Germany
Tel.: +49 7121 35-2979
Fax: +49 7121 35-2170

Robert Bosch Corporation
Component Sales
38000 Hills Tech Drive
Farmington Hills, MI 48331
USA
Tel.: +1 248 876-7441
Fax: +1 248 848-2818

Robert Bosch K.K.
Component Sales
9-1, Ushikubo 3-chome
Tsuzuki-ku, Yokohama 224
Japan
Tel.: +81 45 9 12-83 01
Fax: +81 45 9 12-95 73

E-Mail: bosch.semiconductors@de.bosch.com

Internet: www.bosch-semiconductors.de