Mask Set Errata

MC68HC08AZ32 8-Bit Microcontroller Unit

INTRODUCTION

This document describes the errata identified on mask sets:

G23V, G49V, 0H56A, 1H56A, 0J66D.

The current production mask sets are either 1H56A or 0J66D. Errata not affecting these mask sets are given for information and are in italics.

1) A/D MODULE (REV D) — G23V ONLY

The A/D module draws excessive current, in the order of milli-amps, when it is disabled. This is due to multiple DC paths within the module. To minimise power consumption in WAIT and STOP modes, the A/D module should be enabled. The design fix for this problem has been identified and will be implemented on next silicon (MASK set G49V).

2) LATCH-UP — G23V AND G49V ONLY

Negative latch-up can occur with input trigger currents below the specification of 200mA on all pads dependent upon circuit conditions. If the trigger current is applied to a pad adjacent to a pad which is in output mode driving a logic one then latch-up can occur between the 2 pads. The design fix for this problem has been identified and will be implemented in silicon on the next design revision, which will be MASK set H56A.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

MSE Published Date: September 17, 1999

3) MSCAN MODULE (REV A) — G23V AND G49V ONLY

When an ERROR FRAME occurs in the ARBITRATION FIELD of a Standard Format Frame or in the first half of the ARBITRATION FIELD of an Extended Format Frame and the BUS IDLE field of the INTERFRAME SPACE before the next frame (F) has zero or only a few bits length, and there is no error in the transmission of frame (F), then a receiving node will send a ‘DOMINANT’ bit in the ACK SLOT and set the RXF flag indicating receipt of a valid message. However the data in the FOREGROUND BUFFER will be incorrect.

For Extended Format Frames, the incorrect frame is a left-shifted image of the correct frame. The amount of shifting depends on the position of the ERROR FRAME within the ARBITRATION FIELD. The design fix for this error has been identified and will be implemented in silicon on the next design revision, which will be MASK set H56A.

4) MSCAN MODULE (REV A) — G23V AND G49V ONLY

The MSCAN module on the assertion of the ‘SLEEP REQUEST BIT’ will enter SLEEP mode without waiting for completion of BUS activity. The design fix for this error has been identified and will be implemented in silicon on the next design revision, which will be MASK set H56A.

5) LVI MODULE — G23V AND G49V ONLY

If enabled, the LVI remains enabled in STOP mode, drawing approximately 150–200µA. LVIOUT and LVI Reset cannot be asserted, however, because the digital filter is not clocked and is effectively disabled. A fix for this problem has been identified and will be implemented in silicon on the next design revision which will be Mask set H56A. A full description of the operation of the LVI will be included in the next revision of the HC08AZ0 Technical Summary.

6) EBI MODULE — G23V AND G49V ONLY

When a STOP or WAIT instruction is executed from external memory the MCU enters a low power mode. On current silicon (G23V) the CHIP SELECT (CS0, CS1) and READ/WRITE (REB/WEB) control signals will remain active keeping the external memory active. This can result in excessive current consumption in the application. The CHIP SELECT and READ/WRITE control signals will be inactive during low power modes on the next design revision, MASK set H56A.

Work-around

STOP or WAIT instructions should be executed from internal RAM. This is achieved by copying STOP and WAIT subroutines from external memory in RAM.

In this way, the CHIP SELECT and READ/WRITE signals will be inactive when the STOP instruction is executed and the external memory will be in a low power standby mode.

For example:

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MOV #8E,RAM_LOCATION; copy op-code for STOP
MOV #81,RAM_LOCATION+1; copy op-code for RTS
JSR RAM_LOCATION: jump to STOP instruction.
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7) EMULATOR/TEST MODE — G23V AND G49V ONLY

The EEPROM module is disabled out of reset in TEST/EMULATION mode. This differs from USER MODE in which the EEPROM is enabled out of reset. The operation out of reset of the EEPROM module will be changed to reflect USER mode operation on the next design revision which will be MASK set H56A. The EEPROM can be enabled by writing #$08 to address $FE03, Test Memory Map Control Register out of reset.

8) KEYBOARD MODULE — G23V AND G49V ONLY

The pull-up resistors on pins KBD3 and KBD4 of PORT H have not been connected, therefore an external pull-up must be provided on these 2 pins when they are enabled as Keyboard interrupt pins,.

The fix for this problem has been identified and will be implemented on the next design revision MASK set H56A.

9) MSCAN MODULE — G23V, G49V AND 0H56A

Correct operation of the MSCAN Receive and Transmit Error Counters cannot be assured when running at high temperature across all voltages. The counters can decrement by a count of either 1,2, 3, or 4 due to weak P-channel devices within the error counter control logic. The problem arises when between 1 and 3 errors have occurred in the system. Then after receipt or transmission of a successful message, the error counter decrements by 4 instead of 1, immediately putting the MSCAN module into Receiver Error Passive or Transmitter Error Passive mode. Normal operation will resume once the error counter count returns to below the limit of 127. The P-channel devices have been resized on the1H56A mask set. Special screen tests have been developed for the 0H56A mask set to screen for this failure mode, however samples are very limited due to excessive yield loss. Standard processing is not to screen for this failure.

10) SPI MODULE — G23V, G49V, 0H56A AND 1H56A

The SPI module is affected by a race condition.The problem occurs when the SPI is disabled. Disabling the SPI causes the internal SSB signal to go high. In current versions of the SPI it is possible for this to happen before the SPI has shutdown the Mode Fault detection circuitry, resulting in an invalid Mode Fault.

The fix for this race condition has been simulated but has yet to be implemented on silicon.

Work-around

The problem can be avoided if mode faults are disabled by clearing the MODFEN bit in the SPSCR register before disabling the SPI in slave mode.

11) TIMER MODULES TIMA AND TIMB — G23V, G49V, 0H56A AND 1H56A

When the Toggle on Overflow (TOV) bit is set, writing to a TCHxH register at the point of an overflow inhibits the associated pin from toggling until the TCHxL register is written. The pin will then toggle at the next overflow. Even though a toggle can be completely missed, the TOF flag will be set and an interrupt can be generated.The only thing that should inhibit a toggle on overflow and the setting of the TOF bit, is writing to TMODH register until the TMODL register is written. Similarly, in Buffered PWM mode, writing to the inactive registers (TCH0H:L, TCH2H:L, TCH4H:L) at this overflow point will produce the same problem. Writing to the odd channels (TCH1H:L, TCH3H:L, TCH5H:L) will produce no fault.

The fix for this fault condition has been simulated but has yet to be implemented on silicon.

Work-around

The problem can be avoided by using the overflow routine instead of writing to inactive channel registers within the output compare routine. Each output compare event occurs as a result of the last channel register written to prior to the last overflow.

Make sure that both odd and even timer channel registers are initialised and write to the odd channels last. This is required because, by default, the active channel register on start up is the even channel. Thus, if the inactive channel register is not written to last, then the next PWM pulse width will be exactly the same as the first, reflecting the value written to the even channel register.

12) MSCAN MODULE — G23V, G49V, 0H56A AND 1H56A

In an ‘almost overrun’ condition, the MSCAN receive buffer can contain an incorrect message.The following sequence will cause the receive buffer to have an incorrect message. The message will be a shifted image of the true message:

1) Both foreground & background receive buffers are filled but have not yet been released by software.

2) The MSCAN begins to transmit message ‘M’

3) Software releases one or both receive buffers by clearing RXF bits

4) The MSCAN loses arbitration on the CAN bus while transmitting ‘M’

5) The next bits seen on the bus after clearing RXF will be interpreted as the beginning of the ID field. This ‘shifted’ ID happens to pass the filter configuration programmed into MSCAN

Work-around

The receive driver software must process the incoming stream of messages fast enough to never have the MSCAN enter the state with both buffers filled (almost overrun). When overrun occurs (OVRIF=1), the MSCAN receive queue must be initialized by asserting/deasserting SFTRES. If the software is designed such that it can cope with maximum CAN throughput, this case will never occur.

13) STOP IDD — 1H56A AND 0J56D

Variable Stop IDD currents in Stop Mode may be seen. This is due to a floating node within the A/D converter module. The effect of this floating node is that the total Stop Idd current exceeds the published value of 150µA for LVI disabled over the temperature range –40°C to +125°C after a number of seconds. Typical values seen are between 150µA and 350µA. However, in the case of the LVI being enabled, the specification of 600µA over the temperature range –40°C to +125°C is not exceeded.

Typical data across full temp range worst case supply voltage for samples from 3 wafer lots:

–40°C to 85°C

Mean Stop IDD 123µA
STD Dev 107µA
Mean +3 sigma 553µA
Max recorded value 559µA
Specification 600µA

–40°C to 125°C

Mean Stop IDD 268µA
STD Dev 126µA
Mean +3 sigma 646µA
Max recorded value 559µA
Specification 600µA

14) SIM (SYSTEM INTEGRATION MODULE) — 1H56A AND 0J66D

An illegal address reset is generated when data is accessed in an unimplemented address using indexed addressing mode instructions and PUL/PSH.

This is treated as an internal reset and the RESET pin is driven low for 32 clock cycles.

15) ROM SECURITY — 1H56A AND 0J66D

The ROM security feature is not offered on the 68HC08AZ/AB ROM device because the operation of security in monitor mode does not match that of other HC08 family members.

NOTE: *Only errata items erratum 14 and erratum 15 apply to the 0J66D mask set. All other issues have been addressed by design changes.*

Additional mask set erratas can be found on the World Wide Web at http://mot-sps.com/csic/techhelp/mse/mse.htm.