Product Proposal

HCS12DBFAMILYPP/D
Rev. 0.7, 8/2003

HCS12DB Family Product Proposal

MOTOROLA
intelligence everywhere™

digital dna™

Introduction

Designed for automotive multiplexing applications, members of the MC9S12DB-Family of 16 bit Flash-based microcontrollers are fully pin compatible and enable users to choose between different memory and peripheral options for scalable designs. All MC9S12DB-Family members are composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), up to 128K bytes of Flash EEPROM, 8K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), up to two serial peripheral interfaces (SPI), an enhanced capture timer (ECT), two 8-channel, 10-bit analog-to-digital converters (ADC), an eight-channel pulse-width modulator (PWM), Byteflight interface and up to two CAN 2.0 A, B software compatible modules (MSCAN12). System resource mapping, clock generation, interrupt control and bus interfacing are managed by the system integration module (SIM). The MC9S12DB-Family has full 16-bit data paths throughout, however, the external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, up to 22 I/O ports are available with Wake-Up capability from STOP or WAIT mode.

Table 1. MC9S12DB Family Members

Flash	RAM	EEPROM	Package	Device	CAN	Byte Flight	SCI	SPI	A/D	PWM	I/O
128K	8K	2K	112 LQFP	MC9S12DB128	2	1	2	2	2/16	8 ch	91
			80 QFP		0	1	1	2	1/8	7 ch	59
64K	8K	2K	80 QFP	MC9S12DB64	0	1	1	1	1/8	7 ch	59

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Features

NOTE: *Not all features listed here are available in all configurations.*

- 16-bit CPU12
  - Upward compatible with M68HC11 instruction set
  - Interrupt stacking and programmer's model identical to M68HC11
  - 20-bit ALU
  - Instruction queue
  - Enhanced indexed addressing
- Multiplexed bus
  - Single chip or expanded
  - 16 address/16 data wide or 16 address/8 data narrow modes
  - External address space 1 MB for data and program space (112 pin package only)
- Wake-up interrupt inputs depending on the package option
  - 8-bit port H
  - 4-bit port J
  - 8-bit port shared with PWM/SPI
- Memory options
  - 64K, 128K Byte Flash EEPROM
  - 2K Byte EEPROM
  - 8K Byte RAM
- One or Two analog-to-digital converters (ATD)
  - 1 or 2 times 8-channels, 10-bit resolution depending on the package option
  - External conversion trigger capability
- Up to two 1 M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Enhanced Capture Timer (ECT)
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels; 4 of the 8 input captures with buffer
  - Input capture filters and buffers, three successive captures on four channels, or two captures on four channels with a capture/compare selectable on the remaining four
  - Four 8-bit or two 16-bit pulse accumulators
  - 16-bit modulus down-counter with 4-bit prescaler
  - Four user-selectable delay counters for signal filtering

- Seven or eight PWM channels with programmable period and duty cycle
  - 8-bit 4-channel or 16-bit 2-channel (80-Pin Version)
  - 8-bit 8-channel or 16-bit 4-channel (112-Pin Version)
  - Separate control for each pulse width and duty cycle
  - Center- or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
- Serial interfaces
  - Two asynchronous serial communications interfaces (SCI)
  - Up to two synchronous serial peripheral interfaces (SPI)
- Byteflight
  - 10 MBit/s serial protocol
- SIM (system integration module)
  - CRG (windowed COP watchdog, real-time interrupt, clock monitor, clock generation and reset)
  - MEBI (multiplexed external bus interface)
  - MMC (memory map and interface)
  - INT (interrupt control)
  - BKP (breakpoints)
  - BDM (background debug mode)
- Clock generation
  - Phase-locked loop clock frequency multiplier
  - Limp home mode in absence of external clock
  - Slow mode divider
  - Low power 0.5 to 40 MHz crystal oscillator reference clock
- Operating frequency
  - 50 MHz equivalent to 25 MHz bus speed for single chip
  - 40 MHz equivalent to 20 MHz bus speed in expanded bus modes
- Internal 5 V to 2.5 V regulator
- 112-Pin LQFP or 80-Pin QFP package
  - I/O lines with 5-V input and drive capability
  - 5-V ATD inputs
  - Dual supply (5 V for I/O and ATD, 2.5 V for logic
- Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints

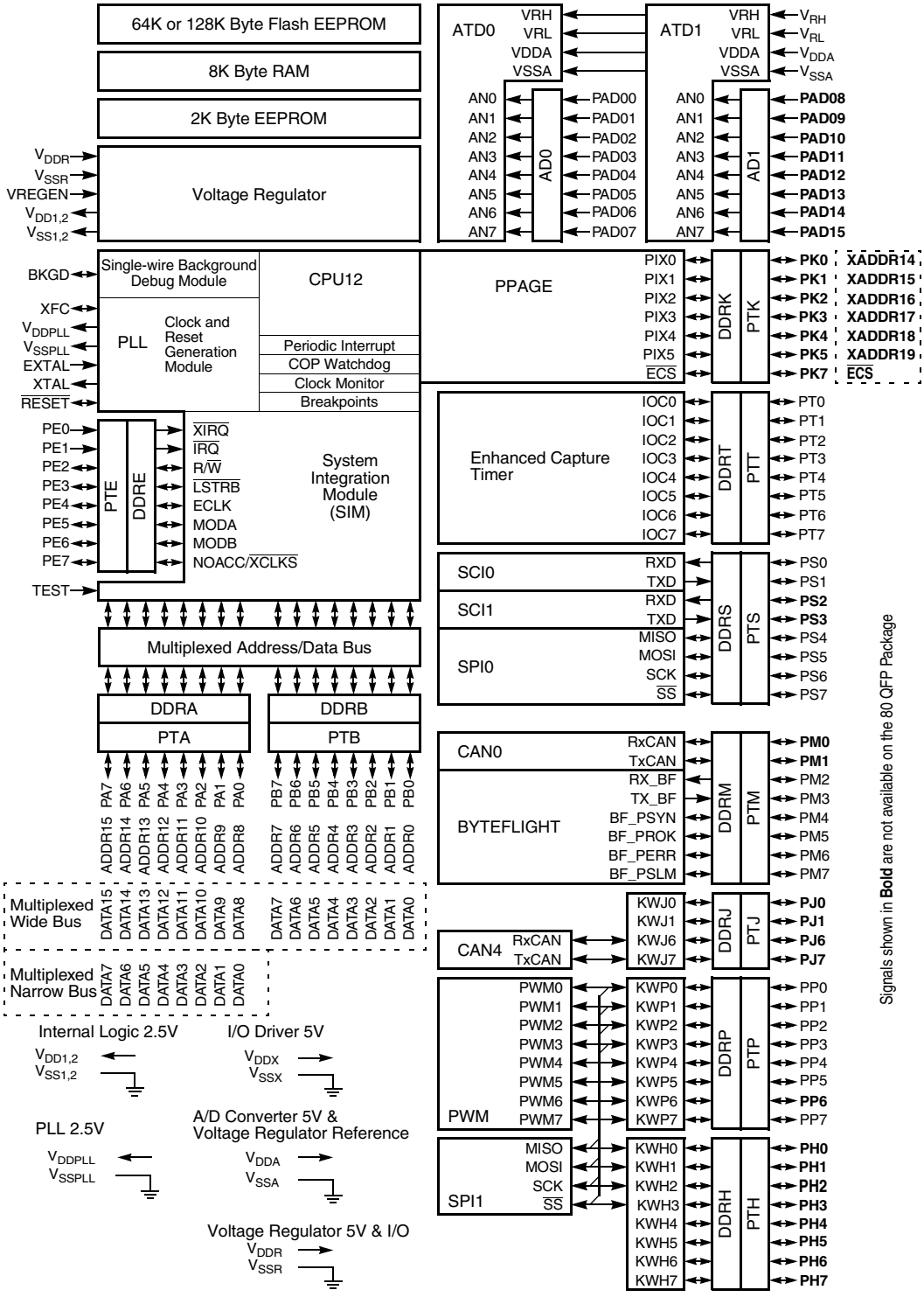
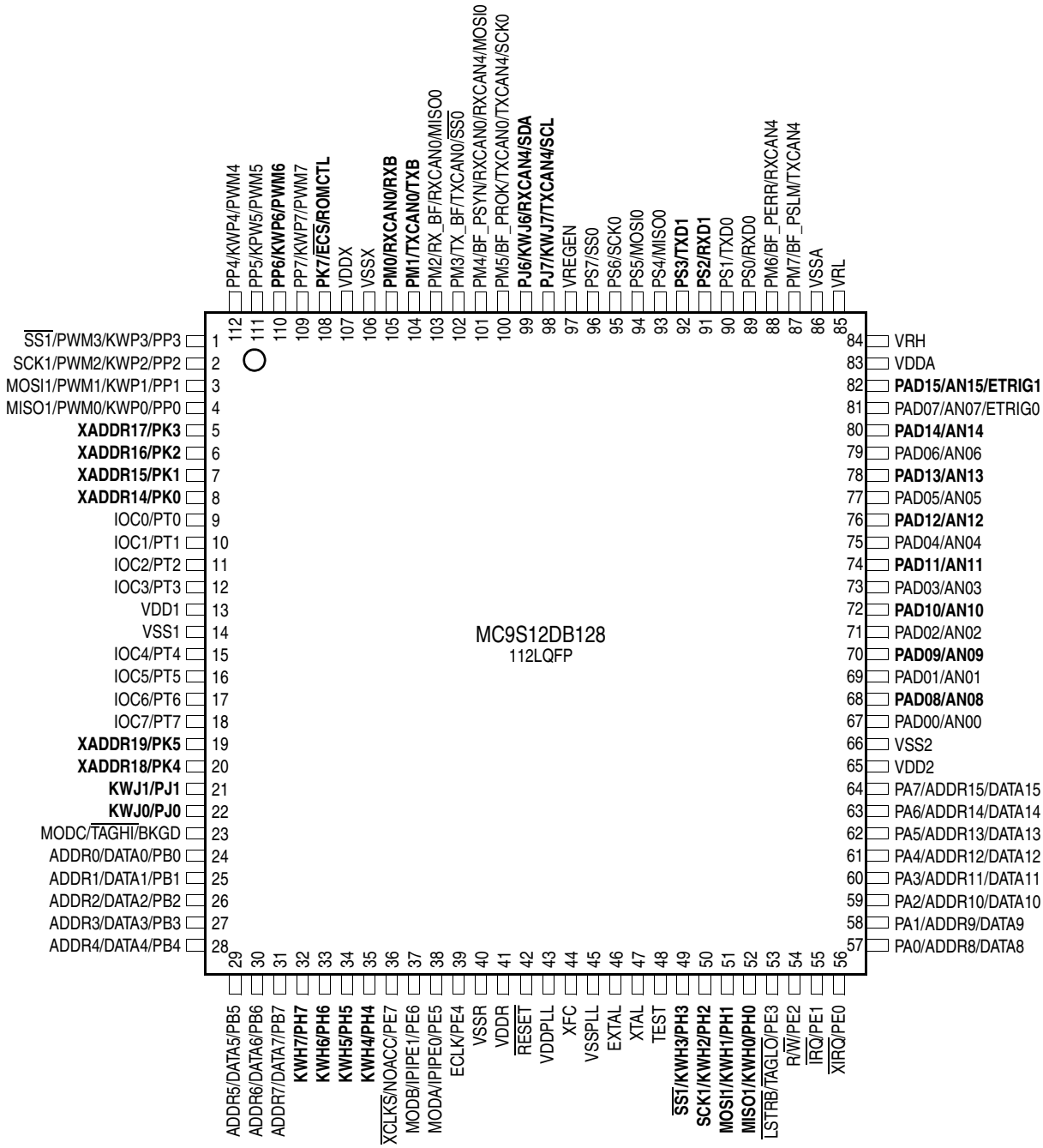


Figure 1. MC9S12DB Family Block Diagram

Pin Out Explanations:

- A/D is the number of modules/total number of A/D channels.
- I/O count:
  - 112 Pin Package:
    - Port A = 8, B = 8, E = 6 + 2 input only, H = 8, J = 4, K = 7, M = 8, P = 8, S = 8, T = 8,
    - PAD = 16 input only.
    - 22 inputs provide Interrupt capability (H =8, P= 8, J = 4, IRQ, XIRQ)
  - 80 Pin Package:
    - Port A = 8, B = 8, E = 6 + 2 input only, M = 6, P = 7, S = 6, T = 8, PAD = 8 input only
    - 9 inputs provide Interrupt capability (P= 7, IRQ, XIRQ)
- MC9S12DB64 features only one SPI, SPI0
- SPI1 pins are shared with PWM3:0 or Port H3:0 routeable under software control



Signals shown in **Bold** are not available on the 80 Pin Package

Figure 2. Pin Assignments 112 LQFP for MC9S12DB128

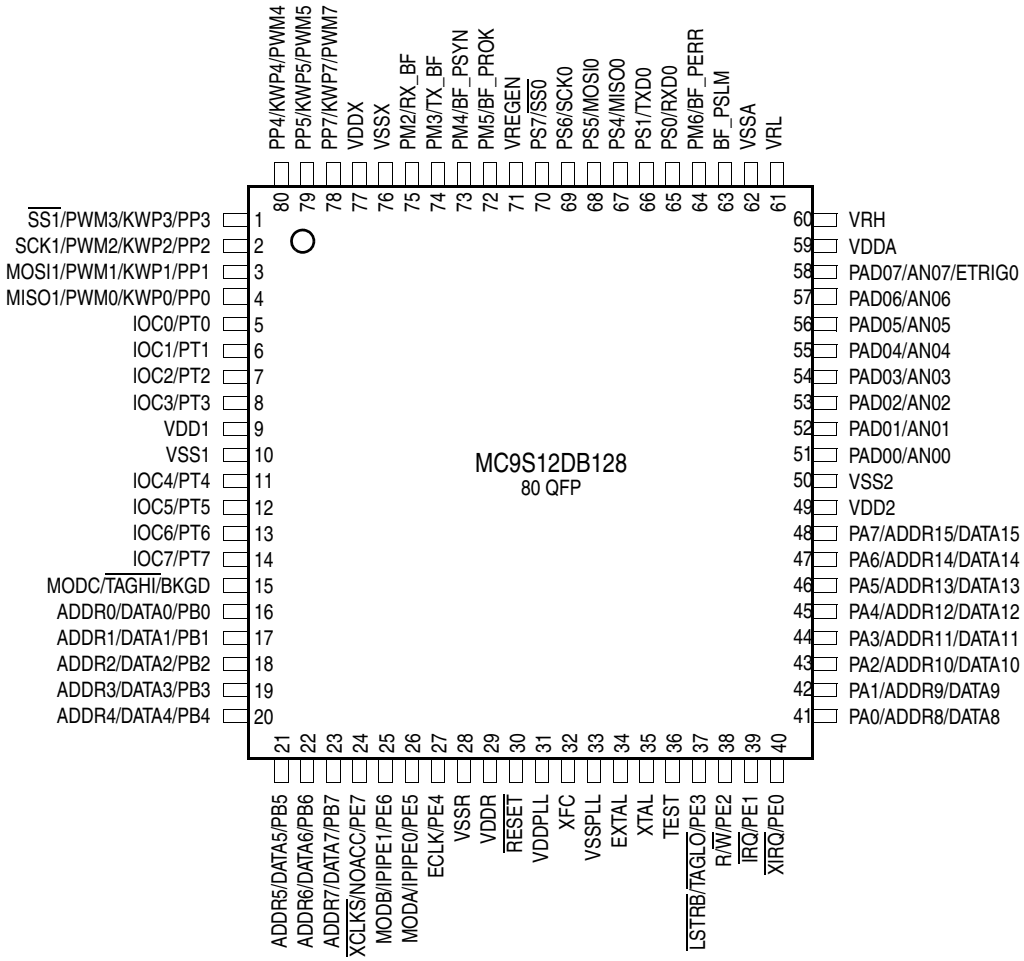


Figure 3. Pin Assignments MC9S12DB128 in 80 QFP

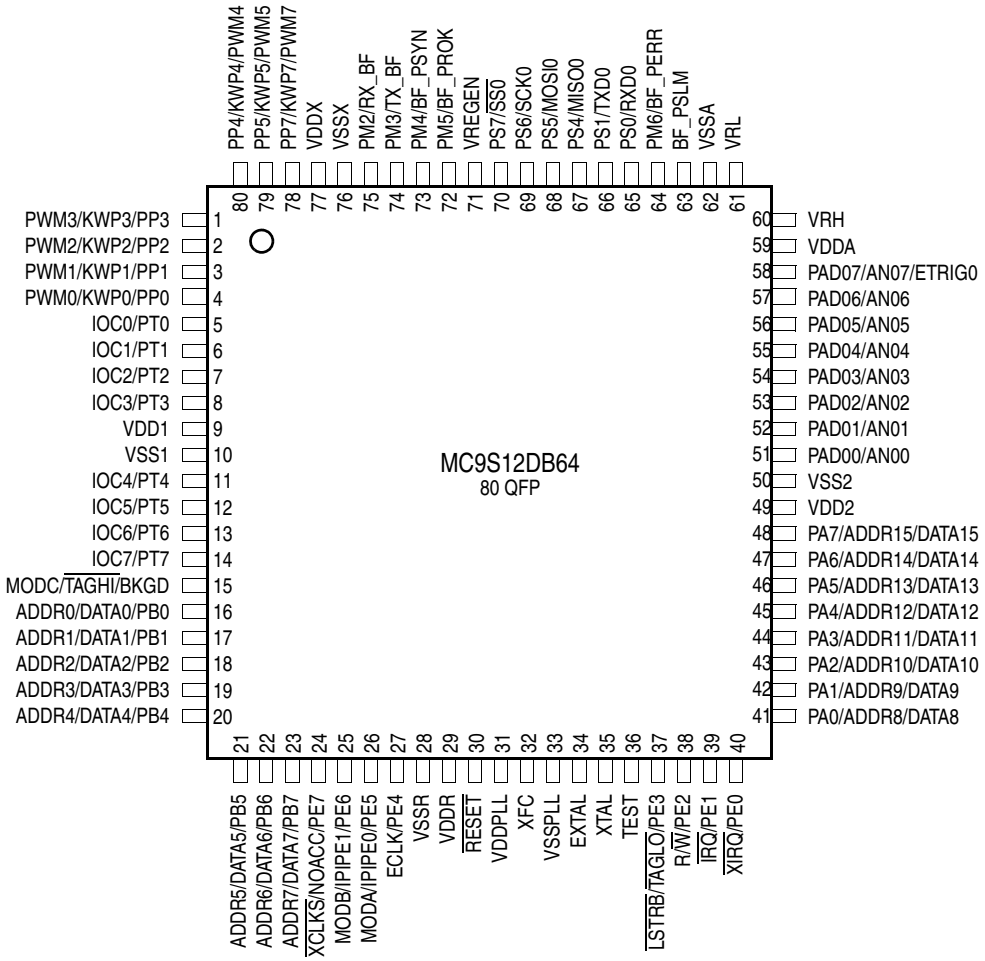
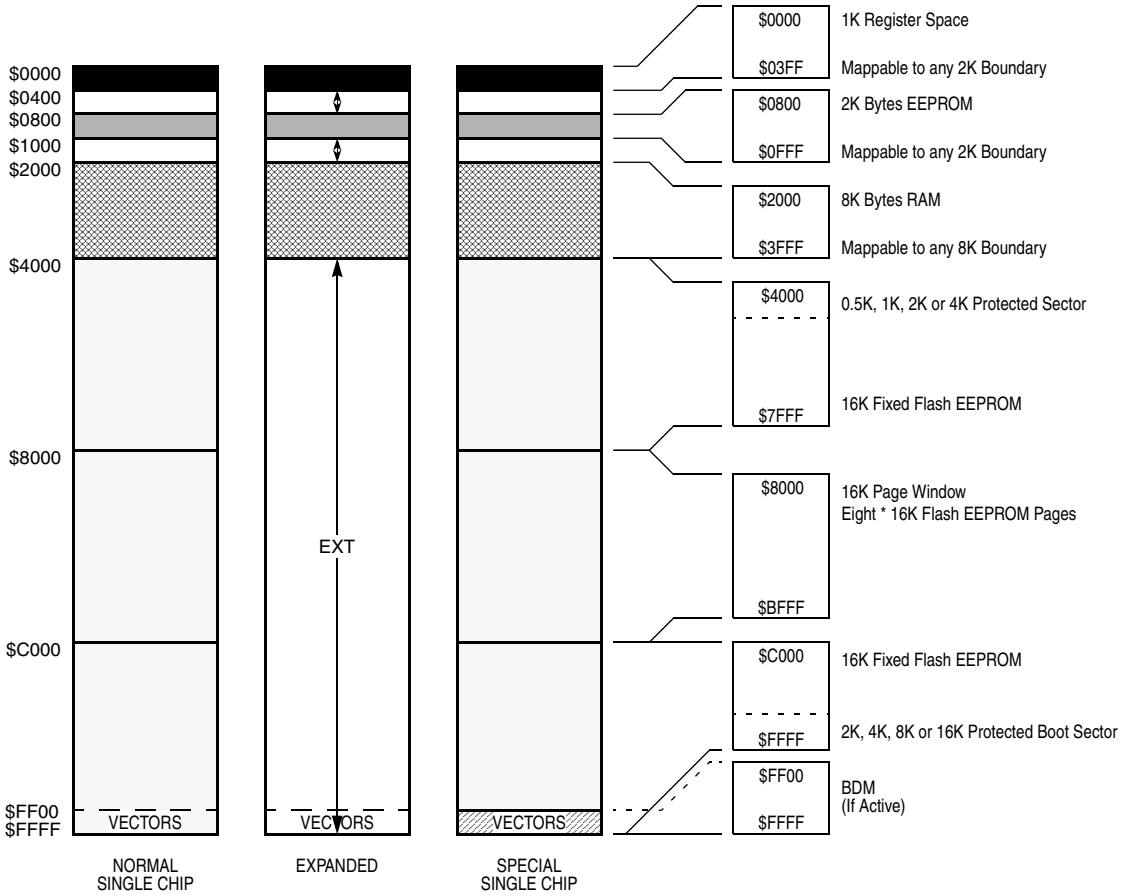
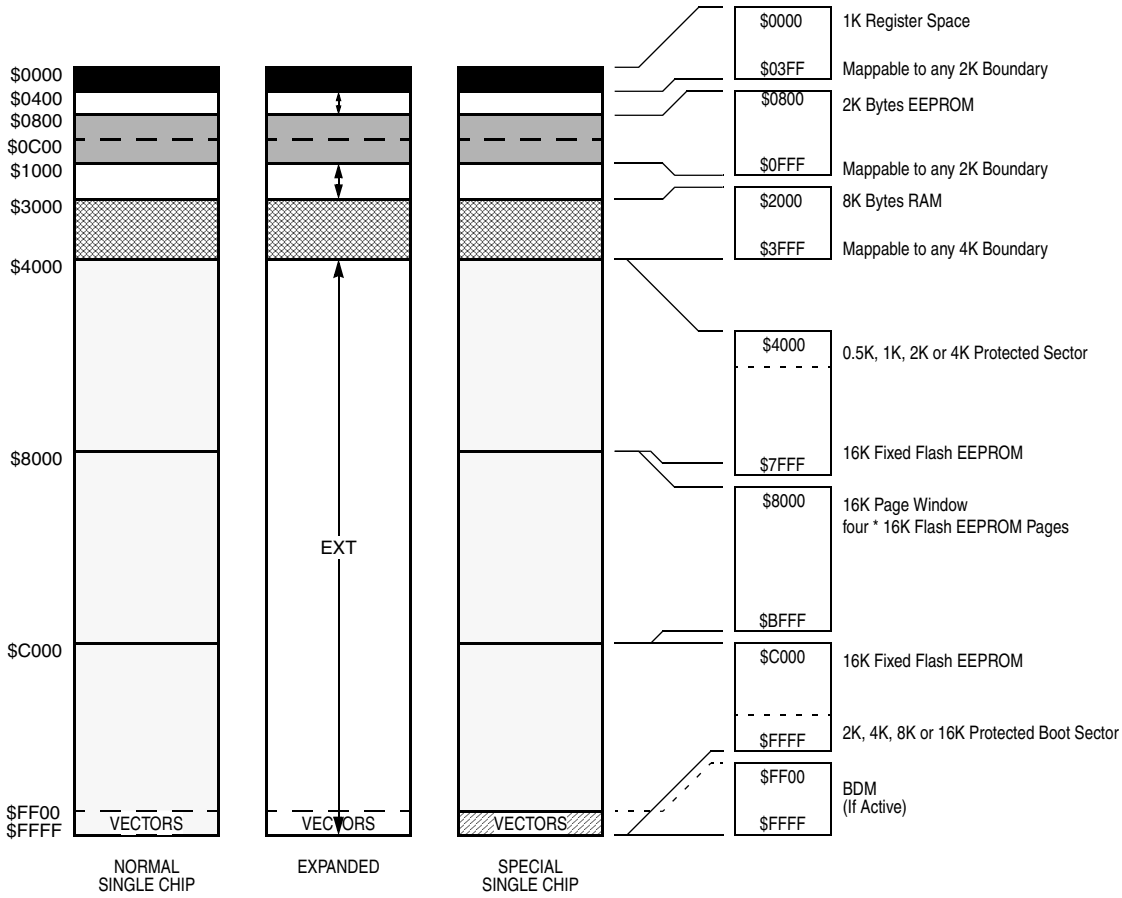


Figure 4. Pin Assignments MC9S12DB64 in 80 QFP



The address does not show the map after reset, but a useful map. After reset the map is:
$0000 - $03FF: Register Space
$0000 - $1FFF: 8K RAM
$0000 - $07FF: 2K EEPROM (not visible)

Figure 5. MC9S12DB128 User Configurable Memory Map



The figure shows a useful map, which is not the map out of reset. After reset the map is:

$0000 - $03FF: Register Space
$0000 - $1FFF: 8K RAM
$0000 - $07FF: 2K EEPROM (not visible)

Figure 6. MC9S12DB64 User Configurable Memory Map

This page intentionally left blank.

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:
Motorola Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

JAPAN:
Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu
Minato-ku
Tokyo 106-8573, Japan
81-3-3440-3569

ASIA/PACIFIC:
Motorola Semiconductors H.K. Ltd.
Silicon Harbour Centre
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T. Hong Kong
852-26668334

HOME PAGE:
http://motorola.com/semiconductors

HCS12DBFAMILYPP/D
Rev. 0.7