MC9S12D64MSE2 Rev 1
September 25, 2002

Mask Set Errata 2

MC9S12D64* Microcontroller Unit

(*Devices covered: MC9S12D64 and MC9S12DJ64)

INTRODUCTION

This errata provides information applicable to the following MCU mask set devices:

- 1L86D

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter, for example F74B. Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code, for example 0F74B.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code “9115” would indicate the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC, PC, ZC or XC prefix. An SC, PC or ZC prefix denotes special/custom device. An XC prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix (or SC for some custom parts).

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

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ERRATA SYSTEM TRACKING NUMBERS

MUCTS00xxx is the tracking number for device errata. It can be used with the mask set and date code to identify a specific errata to a Motorola representative.

ERRATA SUMMARY

Errata Number	Module affected	Brief description	Workaround available?	First Issued
MUCts00628	KWU	Key wake-up: Glitch filter exceeds upper 10µs limit	No	Rev 1
MUCts00636	MSCAN	Glitch filter exceeds spec limits	No	Rev 1
MUCts00681	BDM	Spurious SYNC pulse	Yes	Rev 1
MUCts00692	ESD	ESD fails for 2KV HBM	No	Rev 1
MUCts00708	SPI	SPTEF flag set wrongly	Yes	Rev 1
MUCts00738	ATD	Flags in ATDSTAT0 do not clear by writing "1", ETORF sets wrongly	Yes	Rev 1
MUCts00742	SPI	SPI in mode fault state, but MISO output buffer not disabled	No	Rev 1

KEY WAKE-UP: GLITCH FILTER EXCEEDS UPPER 10µS LIMIT MUCTS00628

The specified maximum limit of the key wake-up glitch filter pulse can be exceeded at high temp/low VDD, i.e. the CPU may not wake up from STOP mode on pulses >=10µs. The device operates at a relaxed limit of 14µs.

Work-around None

MSCAN: GLITCH FILTER EXCEEDS SPEC LIMITS MUCTS00636

The specified MSCAN wake-up glitch filter pulse limits can be exceeded. At low temp/high VDD the module may wake up from sleep mode on glitches <2µs while for pulses >5µs it may not wake up from sleep mode at high temp/low VDD. The device operates at relaxed limits:

MSCAN Wake-up dominant pulse filtered: max. 1µs

MSCAN Wake-up dominant pulse pass: min. 7µs

Work-around None

SPURIOUS SYNC PULSE MUCTS00681

A spurious BDM SYNC pulse could be transmitted if the delay between commands is such that the first negative edge of a new command occurs exactly 128 cycles after the last negative edge of the previous command.

Work-around Keep the delay between commands greater than 128 cycles.

ESD FAILS FOR 2KV HBM MUCTS00692

ESD performance:

- 2KV HBM (Human Body Model) fails ESD tests
- 1.75KV HBM pass ESD tests

Therefore, reduced ESD spec for HBM is 1.75KV

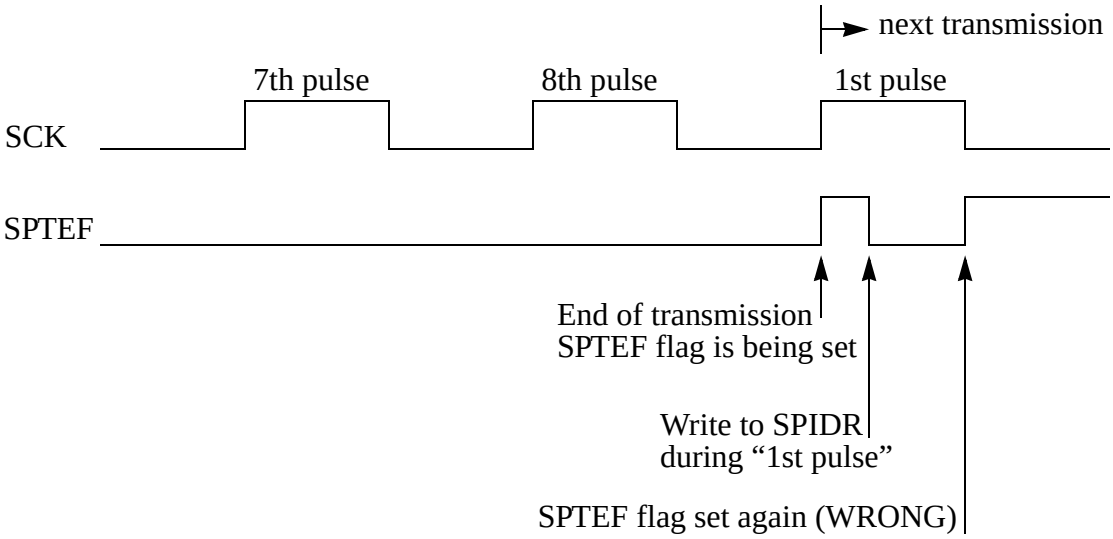
Work-around None

SPTEF FLAG SET WRONGLY MUCTS00708

When the SPI is enabled in master mode, with the CPHA bit set, back to back transmissions are possible.

When a transmission completes and a further byte is available in the SPI Data Register, the second transmission begins directly after the “minimum trailing time”.

The problem occurs when, after the SPTEF flag has been set, a further byte is written into the SPI Data Register during the “1st pulse” of a subsequent transmission.



Then the SPTEF flag is set at the falling SCK edge of the “1st pulse” and data is transferred from the SPI Data Register to the transmit shift register. The result is that the transmission is corrupted and data is lost.

Work-around

After the SPTEF flag has been set, a delay of 1/2 SCK period has to be added before storing data into the SPI Data Register.

ATD: FLAGS IN ATDSTAT0 DO NOT CLEAR BY WRITING ‘1’, ETORF SETS WRONGLY MUCTS00738

For the flags SCF, ETORF and FIFOR in ATDSTAT0 it is specified that: Write ‘1’ to the respective flag clears it. This does not work. Writing ‘1’ to the respective flag has no effect. The ETORF flag is also set by a non active edge, e.g. falling edge trigger (ETRILE=0, ETRIGP=0). ETORF is set on both falling edges and rising edges while conversion is in progress.

Work-around

SCF

1. Use the alternative flag clearing mechanisms:
   a. Write to ATDCTL5 (a new conversion sequence is started)
   b. If AFFC=1 and read of a result register

ETORF

1. Use the alternative flag clearing mechanisms:
   a. Write to ATDCTL2, ATDCTL3 or ATDCTL4 (a conversion sequence is aborted)
   b. Write to ATDCTL5 (a new conversion sequence is started)
2. Avoid external trigger edges during conversion process by using short pulses
3. Ignore ETROF flag

FIFOR

1. Use the alternative flag clearing mechanism:
   a. Start a new conversion sequence (write to ATDCTL5 or external trigger)

SPI: SPI IN MODE FAULT STATE, BUT MISO OUTPUT BUFFER NOT DISABLED MUCTS00742

When the SPI is in Mode Fault state (MODF flag set), according to the specification, all SPI output buffers (SS, SCK, MOSI, MISO) should be disabled. However, the MISO output buffer is not disabled.

Work-around

None

Additional mask set errata can be found on the World Wide Web at http://www.mcu.motsps.com/documentation/index.html