27C256

256K (32K x 8) CMOS EPROM

FEATURES

- High speed performance
  - 90 ns access time available
- CMOS Technology for low power consumption
  - 20 mA Active current
  - 100 μA Standby current
- Factory programming available
- Auto-insertion-compatible plastic packages
- Auto ID aids automated programming
- Separate chip enable and output enable controls
- High speed "express" programming algorithm
- Organized 32K x 8: JEDEC standard pinouts
  - 28-pin Dual-in-line package
  - 32-pin PLCC Package
  - 28-pin SOIC package
  - 28-pin Thin Small Outline Package (TSOP)
  - 28-pin Very Small Outline Package (VSOP)
  - Tape and reel
- Data Retention > 200 years
- Available for the following temperature ranges:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

DESCRIPTION

The Microchip Technology Inc. 27C256 is a CMOS 256K bit electrically Programmable Read Only Memory (EPROM). The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 90 ns. This very high speed device allows the most sophisticated micro-processors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. For surface mount appli-cations, PLCC, SOIC, VSOP or TSOP packaging is available. Tape and reel packaging is also available for PLCC or SOIC packages.

PACKAGE TYPES

27C256
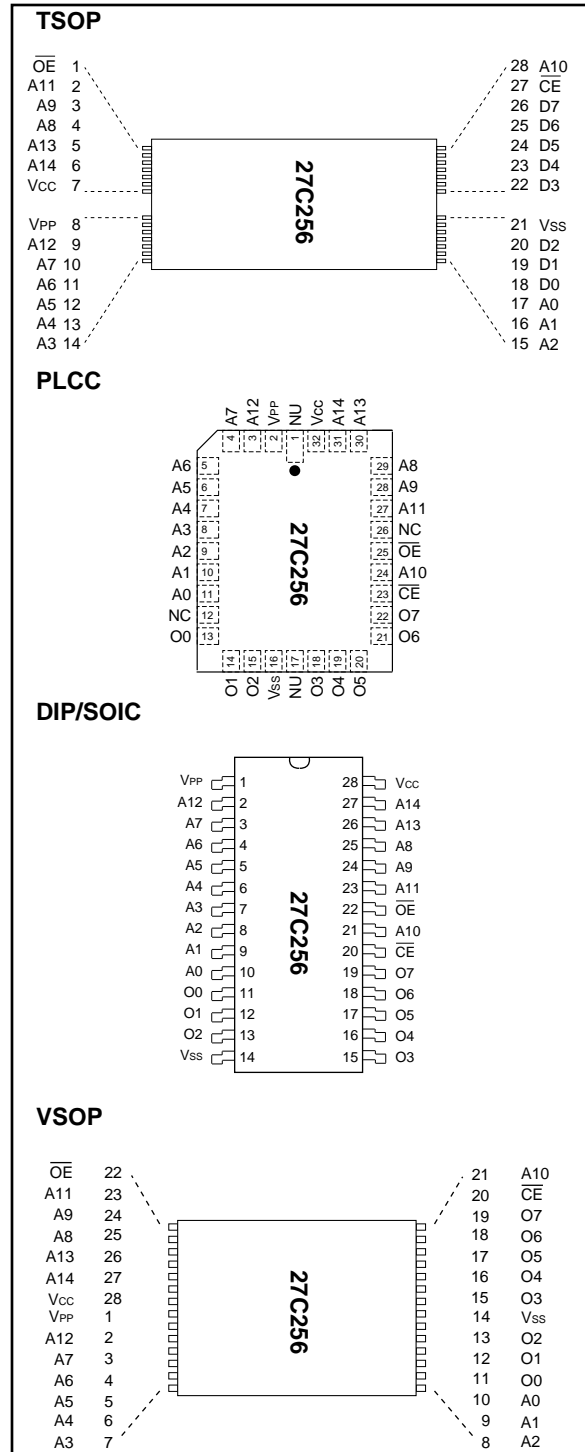
1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc and input voltages w.r.t. Vss .... -0.6V to +7.25V

Vpp voltage w.r.t. Vss during
programming .... -0.6V to +14.0V

Voltage on A9 w.r.t. Vss .... -0.6V to +13.5V

Output voltage w.r.t. Vss .... -0.6V to Vcc +1.0V

Storage temperature .... -65˚C to +150˚C

Ambient temp. with power applied ..... -65˚C to +125˚C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
Vpp	Programming Voltage
O0 - O7	Data Output
Vcc	+5V Power Supply
Vss	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection Is Allowed

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

				Vcc = +5V (±10%) Commercial: Tamb = 0˚C to +70˚C Industrial: Tamb = -40˚C to +85˚C Extended (Automotive): Tamb = -40°C to +125°C			
Parameter	**Part***	**Status**	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	Vcc+1 0.8	V V	
Input Leakage	all	—	ILI	-10	10	µA	VIN = 0 to Vcc
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	0.45	V V	IOH = -400 µA IOL = 2.1 mA
Output Leakage	all	—	ILO	-10	10	µA	VOUT = 0V to Vcc
Input Capacitance	all	—	CIN	—	6	pF	VIN = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	COUT	—	12	pF	VOUT = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	C I,E	TTL input TTL input	ICC1 ICC2	— —	20 25	mA mA	Vcc = 5.5V; Vpp = Vcc f = 1 MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; IOUT = 0 mA; VIL = -0.1 to 0.8V; VIH = 2.0 to Vcc; Note 1
Power Supply Current, Standby	C I, E all	TTL input TTL input CMOS input	ICC(S)	—	2 3 100	mA mA µA	$\overline{CE}$ = Vcc ± 0.2V
IPP Read Current VPP Read Voltage	all all	Read Mode Read Mode	IPP VPP	Vcc-0.7	100 Vcc	µA V	VPP = 5.5V

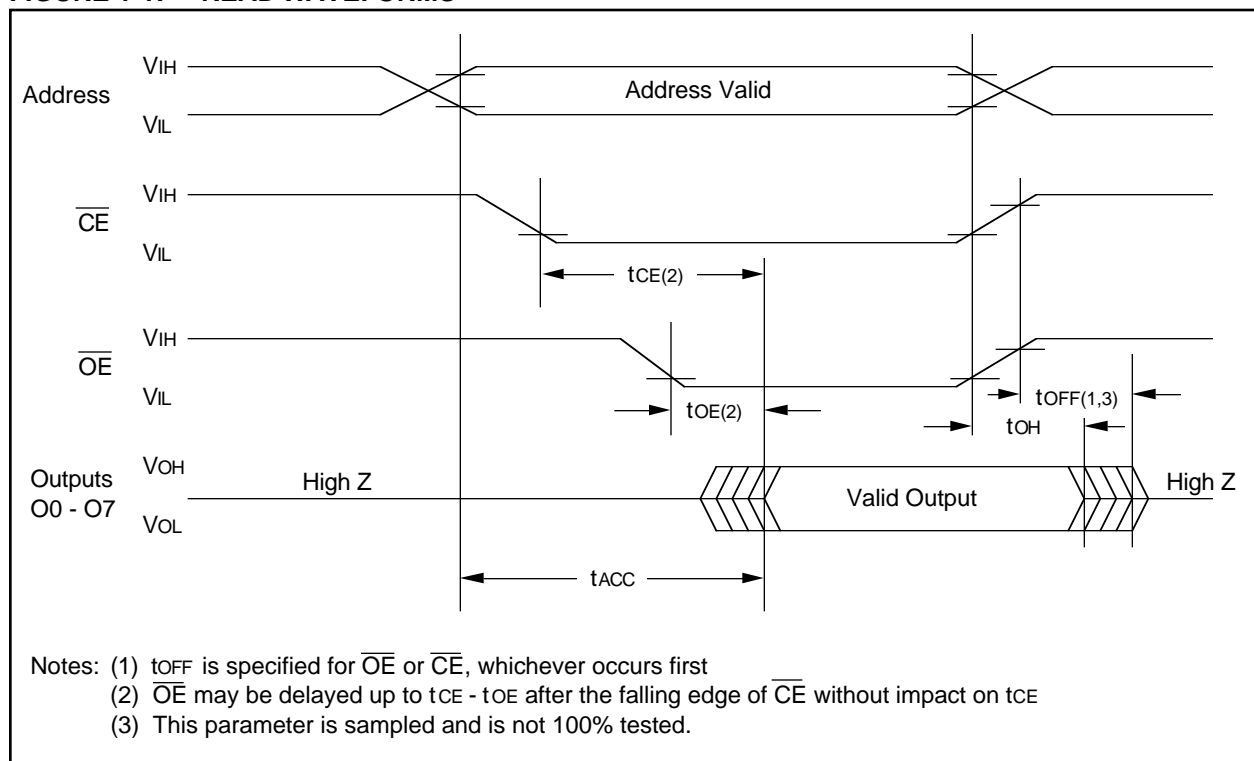* Parts: C=Commercial Temperature Range; I, E=Industrial and Extended Temperature Ranges
Note 1: Typical active current increases .75 mA per MHz up to operating frequency for all temperature ranges.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform:				V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} = 0.8V									
Output Load:				1 TTL Load + 100 pF									
Input Rise and Fall Times:				10 ns									
Ambient Temperature:				Commercial:			Tamb = 0˚C to +70˚C						
				Industrial:			Tamb = -40˚C to +85˚C						
				Automotive:			Tamb = -40°C to +125°C						

Parameter	Sym	27C256-90*		27C256-10*		27C256-12		27C256-15		27C256-20		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	t_{ACC}	—	90	—	100	—	120	—	150	—	200	ns	$\overline{CE}=\overline{OE}=V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}	—	90	—	100	—	120	—	150	—	200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to Output Delay	t_{OE}	—	40	—	45	—	55	—	65	—	75	ns	$\overline{CE} = V_{IL}$
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	t_{OFF}	0	30	0	30	0	35	0	50	0	55	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	t_{OH}	0	—	0	—	0	—	0	—	0	—	ns	

* -10, -90 AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = .45V; V_{OH} = 1.5V and V_{OL} = 1.5V
Output Load: 1 TTL Load + 30pF

FIGURE 1-1: READ WAVEFORMS

Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

27C256

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

						Ambient Temperature: Tamb = 25°C ± 5°C V_{CC} = 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V
Parameter	**Status**	**Symbol**	**Min**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic"1" Logic"0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	—	I_{LI}	-10	10	μA	V_{IN} = 0V to V_{CC}
Output Voltages	Logic"1" Logic"0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = -400 μA I_{OL} = 2.1 mA
V_{CC} Current, program & verify	—	I_{CC2}	—	20	mA	Note 1
V_{PP} Current, program	—	I_{PP2}	—	25	mA	Note 1
A9 Product Identification	—	V_H	11.5	12.5	V	

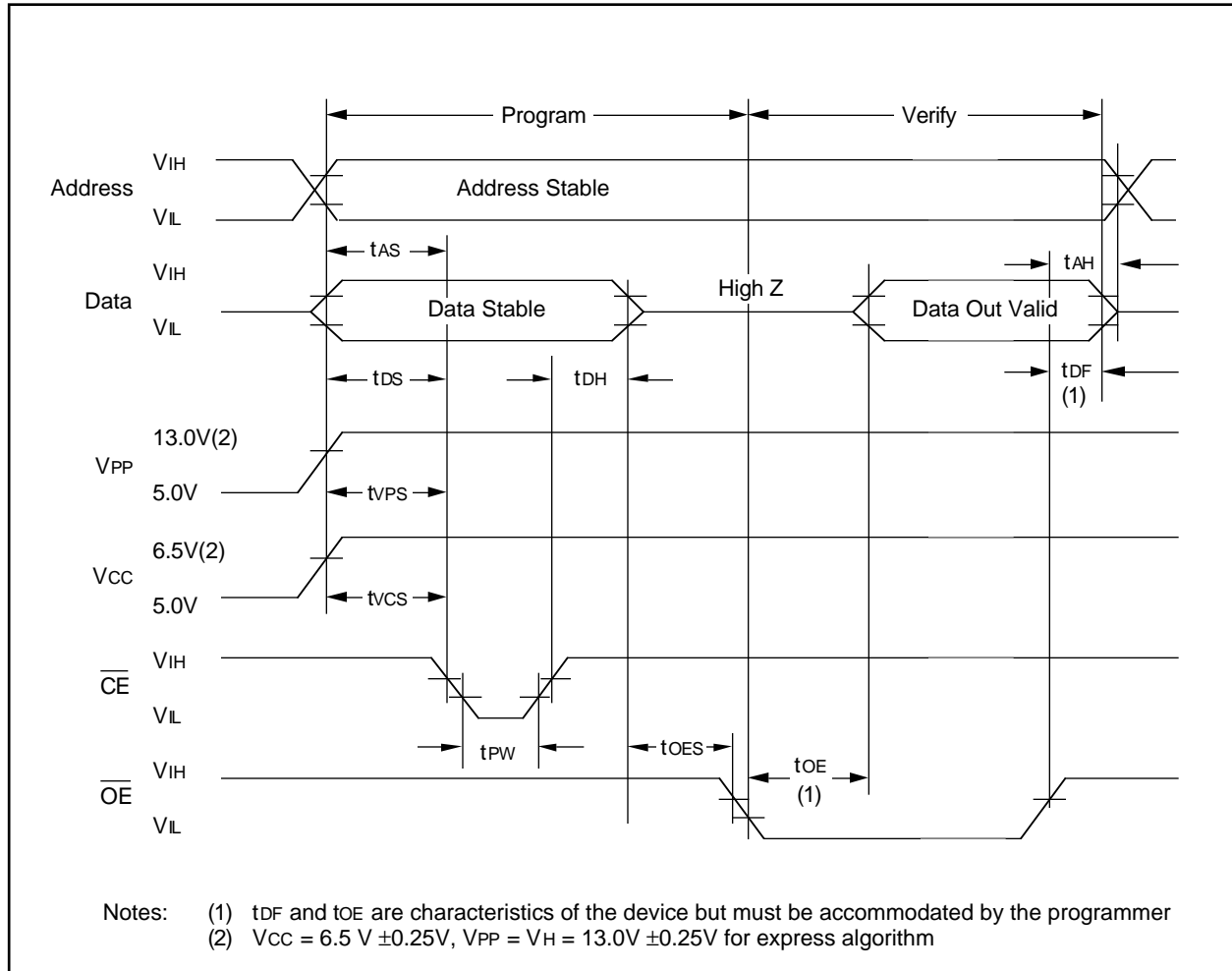Note 1: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: V_{IH}=2.4V and V_{IL}=0.45V; V_{OH}=2.0V; V_{OL}=0.8V Output Load: 1 TTL Load + 100pF Ambient Temperature: Tamb=25°C ± 5°C V_{CC}= 6.5V ± 0.25V, V_{PP} = V_H = 13.0V ± 0.25V					
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Remarks**	
Address Set-Up Time	t_{AS}	2	—	μs		
Data Set-Up Time	t_{DS}	2	—	μs		
Data Hold Time	t_{DH}	2	—	μs		
Address Hold Time	t_{AH}	0	—	μs		
Float Delay (2)	t_{DF}	0	130	ns		
V_{CC} Set-Up Time	t_{VCS}	2	—	μs		
Program Pulse Width (1)	t_{PW}	95	105	μs	100 μs typical	
$\overline{CE}$ Set-Up Time	t_{CES}	2	—	μs		
$\overline{OE}$ Set-Up Time	t_{OES}	2	—	μs		
V_{PP} Set-Up Time	t_{VPS}	2	—	μs		
Data Valid from $\overline{OE}$	t_{OE}	—	100	ns		

Note 1: For express algorithm, initial programming width tolerance is 100 μs ±5%.
2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS

Notes: (1) t_{DF} and t_{OE} are characteristics of the device but must be accommodated by the programmer
(2) V_{CC} = 6.5 V ±0.25V, V_{PP} = V_H = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	OE	VPP	A9	O0 - O7
Read	V_{IL}	V_{IL}	V_{CC}	X	D_{OUT}
Program	V_{IL}	V_{IH}	V_H	X	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_H	X	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_H	X	High Z
Standby	V_{IH}	X	V_{CC}	X	High Z
Output Disable	V_{IL}	V_{IH}	V_{CC}	X	High Z
Identity	V_{IL}	V_{IL}	V_{CC}	V_H	Identity Code

X = Don't Care

1.2 Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when:

a) the $\overline{CE}$ pin is low to power up (enable) the chip
b) the $\overline{OE}$ pin is low to gate the data to the output pins

For Read operations, if the addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (t_{OE}).

27C256

1.3 Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (VIH) and a program mode is not defined.

When these conditions are met, the supply current will drop from 20 mA to 100 μA.

1.4 Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

• The $\overline{OE}$ pin is high and the program mode is not defined.

1.5 Erase Mode (U.V. Windowed Versions)

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state when exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm^2 is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000μW/cm^2 for approximately 20 minutes.

1.6 Programming Mode

The Express Algorithm has been developed to improve on the programming throughput times in a production environment. Up to ten 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the express algorithm is shown in Figure 1-3.

Programming takes place when:

a) VCC is brought to the proper voltage,
b) VPP is brought to the proper VH level,
c) the $\overline{OE}$ pin is high, and
d) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that location.

1.7 Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) VCC is at the proper level,
b) VPP is at the proper VH level,
c) the $\overline{CE}$ line is high, and
d) the $\overline{OE}$ line is low.

1.8 Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

1.9 Identity Mode

In this mode specific data is output which identifies the manufacturer as Microchip Technology Inc. and device type. This mode is entered when Pin A9 is taken to VH (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at VIL. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin ⟶	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	VIL	0	0	1	0	1	0	0	1	29
Device Type*	VIH	1	0	0	0	1	1	0	0	8C

* Code subject to change

FIGURE 1-3:   PROGRAMMING EXPRESS ALGORITHM

Conditions:
$T_{amb} = 25°C \pm 5°C$
$V_{CC} = 6.5 \pm 0.25V$
$V_{PP} = 13.0 \pm 0.25V$

Start

ADDR = First Location
$V_{CC} = 6.5V$
$V_{PP} = 13.0V$

X = 0

Program one 100 µs pulse
Increment X

Verify
Byte — Pass

Fail

X = 10 ? — No
Yes — Device Failed

Last
Address? — Yes

No

Increment Address

$V_{CC} = V_{PP} = 4.5V, 5.5V$

All
bytes
= original
data? — Yes — Device Passed
No — Device Failed
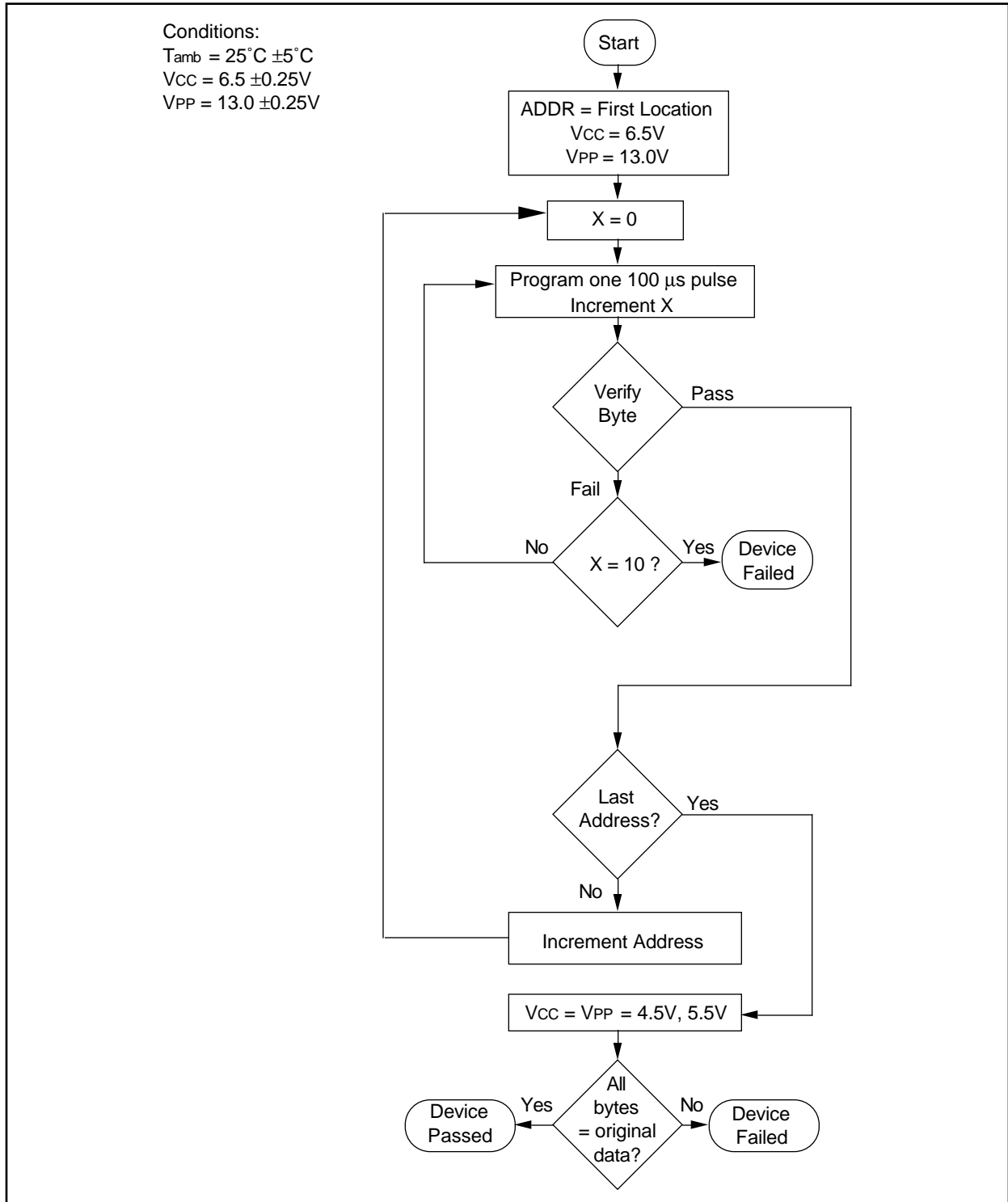
27C256

27C256 Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use listed part numbers, and refer to factory or listed sales offices.

27C256 – 90 I /TS

Package:
- L = Plastic Leaded Chip Carrier
- P = Plastic DIP (Mil 600)
- SO = Plastic SOIC (Mil 300)
- TS = Thin Small Outline Package (TSOP) 8x20mm
- VS = Very Small Outline Package (VSOP) 8x13.4mm

Temperature Range:
- Blank = 0˚C to +70˚C
- I = -40˚C to +85˚C
- E = -40˚C to +125˚C

Access Time:
- 90 = 90 ns
- 10 = 100 ns
- 12 = 120 ns
- 15 = 150 ns
- 20 = 200 ns

Device 27C256 256K (32K x 8) CMOS EPROM